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Gate engineered heterostructure junctionless TFET with Gaussian doping profile for ambipolar suppression and electrical performance improvement

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Abstract

This study investigates a junctionless tunnel field-effect transistor with a dual material gate and a heterostructure channel/source interface (DMG-H-JLTFET). We find that using the heterostructure interface improves device behavior by reducing the tunneling barrier width at the channel/source interface. Simultaneously, the dual material gate structure decreases ambipolar current by increasing the tunneling barrier width at the drain/channel interface. The performance of the device is analyzed based on the energy band diagram at on, off, and ambipolar states. Numerical simulations demonstrate improvements in I_{ON} , I_{OFF} , I_{ON}/I_{OFF} , subthreshold slope (SS), transconductance and cut-off frequency and suppressed ambipolar behavior. Next, the workfunction optimization of dual material gate is studied. It is found that if appropriate workfunctions are selected for tunnel and auxiliary gates, the JLTFET exhibits considerably improved performance. We then study the influence of Gaussian doping distribution at the drain and the channel on the ambipolar performance of the device and find that a Gaussian doping profile and a dual material gate structure remarkably reduce ambipolar current. Gaussian doped DMG-H-JLTFET, also exhibits enhanced I_{OFF} , I_{ON}/I_{OFF} , SS and a low threshold voltage without degrading I_{OFF} .

Keywords: Junctionless tunnel field-effect transistor; Ambipolar Current; Gaussian doping; Heterostructure

1. Introduction

Tunnel field-effect transistors (TFETs) have gained considerable interest for their low subthreshold slope (SS) and low off-state current [1, 2, 3]. These transistors are also reported as energy-efficient and scalable devices [4, 5, 6]. The SS of conventional metal-oxide-semiconductor FETs (MOSFETs) is limited to values greater than 60 mV/dec (2.3 kT/q), which does not ensure a high on-off current ratio

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