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Analog/RF performance of two tunnel FETs with symmetric structures

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ABSTRACT

In this paper, the radio frequency and analog performance of two tunnel field-effect transistors with symmetric structures are analyzed. The symmetric U-shape gate tunnel field-effect transistor (SUTFET) and symmetric tunnel field-effect transistor (STFET) are investigated by Silvaco Atlas simulation. The basic electrical properties and the parameters related to frequency and analog characteristics are analyzed. Due to the lower off-state leakage current, the STFET has better power consumption performance. The SUTFET obtains larger operating current (242 μA/μm), transconductance (490 μS/μm), output conductance (494 μS/μm), gain bandwidth product (3.2 GHz) and cut-off frequency (27.7 GHz). The simulation result of these two devices can be used as a guideline for their analog/RF applications.

1. Introduction

With the scaling down of the metal oxide semiconductor field-effect transistor (MOSFET), the density, power consumption, switching speed of Integrated circuit (IC) has ushered in a great progress [1,2]. However, the performance and reliability degradation caused by short channel effect (SCEs) and off-state leakage current (I_{off}) becomes a serious reliability issue [2–4]. Tunnel field-effect transistor (TFET) has become a promising candidate for future ultralow power and high frequency applications [2,5–8] due to its low I_{off}, steep subthreshold swing (*SS*) [9–12] and robustness of SCE [13]. In order to further improve the performance of TFET, many researchers take measures such as new device structures and materials to improve the on-state current of TFET [14–18]. However, its inherent disadvantage of the asymmetric current path will increase the difficulty of the circuit design. Novel structures, such as symmetric tunnel field-effect transistor (STFET) have been reported to overcome this inborn disadvantage [19,20]. In our previous work, a symmetric U-shape gate tunnel field-effect transistor (SUTFET) with bidirectional current path and enhanced device performance is obtained [21]. Although the DC characteristics of these two devices have already been studied, few efforts were made on the analog/RF performance.

In this paper, for the first time, the analog/RF performance of STFET and SUTFET is studied. The operating current (I_{on}), gate capacitance (C_{gg}), transconductance (g_m), output conductance (g_{ds}), gain bandwidth product (*GBW*) and cut-off frequency (f_T) of these two devices are compared and analyzed.

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The content distribution of this paper is as follows: Section 2 includes the description of the parameters and the structures of STFET and SUTFET, as well as the simulation methods. Section 3 includes the simulation results of STFET and SUTFET. In this section, the analog/RF performance of STFET and SUTFET are compared. Section 4 gives a conclusion of this paper.

2. Device structure

The structures of SUTFET and STFET are illustrated in Fig. 1. In order to form the bidirectional current path, both of these two devices have the symmetric germanium source/drain. The Si/Ge valence band gap can suppress the I_{off} by preventing holes flow from drain to channel in off-state. Thus, In order to suppress the I_{off}, the Si/Ge heterojunction is necessary. In SUTFET, the recessed channel and n + Si pocket are introduced to increase the I_{on}; the stack of n-channel and p-pad are introduced to decrease the I_{off}. In STFET, the p-pad is introduced to be a part of the current path of I_{on}.

In this work, the two devices mentioned above are studied using Silvaco Atlas tool. By the small signal AC simulation at an operating frequency of 1 MHz, the analog and RF performance of SUTFET and STFET are investigated and analyzed. The best candidate for analog/RF application is obtained. The simulation parameters are shown in Table 1.

Simulations of the SUTFET and the STFET are carried out in Silvaco Atlas TCAD tools. Non-local BTBT Model is applied in this simulation to bring the energy band spatial variation into account, which can help to facilitate the accuracy of the BTBT tunneling process. In order to calculate the tunneling current of Si-Ge heterojunction accurately, the indirect tunneling mechanism must be taken into account. Thus, Kane's model is used and the A/B parameters are set as 4.0×10^{14} $cm^{-1}s^{-1}$/ 9.9×10^{6} V/cm for Si and 3.1×10^{16} $cm^{-1}s^{-1}$/7.1×10^{5} V/cm for Ge [22]. Lombardi Mobility Model is considered to make the channel mobility more accurate (by considering the surface scattering caused by the transverse field and doping concentration). Fermi Statistics and Band-gap Narrowing Model are considered to fit the effect of the highly doped regions. Shockley-Read-Hall Recombination Model is also considered in this paper.

3. Simulation and discussion

Fig. 2 (a) shows the transfer characteristics for the SUTFET and STFET at $V_{DS} = 1$ V. The SUTFET has greater I_{on} (242 μA/μm) and steeper *SS* (34mV/dec) than that of the STFET (91 μA/μm and 47mV/dec). This is because that the recessed channel and n + pocket in SUTFET change the band-to-band tunneling area from dot to line, as explained after a few paragraphs. Thus, the area of tunneling junction is increased, which results in the greater I_{on} and steeper *SS*. The I_{off} of the SUTFET is one order of magnitude larger than that of the STFET. This is because the large supply voltage ($V_{DS} = 1$ V) caused drain induced barrier lowering (DIBL), which leads to the intensified hole thermal excitation process in p- Si Pad of SUTFET. Fig. 2 (b) shows the g_m of the SUTFET and STFET. As an important parameter to evaluate analog performance, g_m is defined as the first derivative of the transfer characteristic curve [23] and expressed by Equation (1):

$$g_m = dI_{ds}/dV_{gs} \tag{1}$$

The g_m of two devices increase with the increasing V_g from 0 V to 0.8 V and the maximum value is obtained at V_g~0.8 V. Due to the definition of g_m, the large I_{on} is more advantageous in g_m. Therefore, the SUTFET has greater g_{mmax} (490 μS/μm) than that of the STFET (226 μS/μm).

Fig. 3 (a) shows the output characteristics of SUTFET and STFET. As we already discussed previously, benefit from the greater tunneling junction area, SUTFET has a greater I_{on}. Both SUTFET and STFET are not saturated at $V_g = V_d = 1$ V. Fig. 3 (b) shows the g_{ds} and output resistance (R_o) of these two devices separately. The SUTFET reaches the maximum g_{ds} (494 μS/μm) at V_d~0.85 V, but the STFET does not reach the maximum value even at $V_d = 1$ V. The R_o shown in Fig. 3 (b) is the inverse of g_{ds}, which is determined by the channel resistance and tunneling resistance [24]. As a result, the SUTFET exhibits a larger g_{ds} (and smaller R_o), which is an important parameter to evaluate the device performance. It can be expressed by Equation (2):

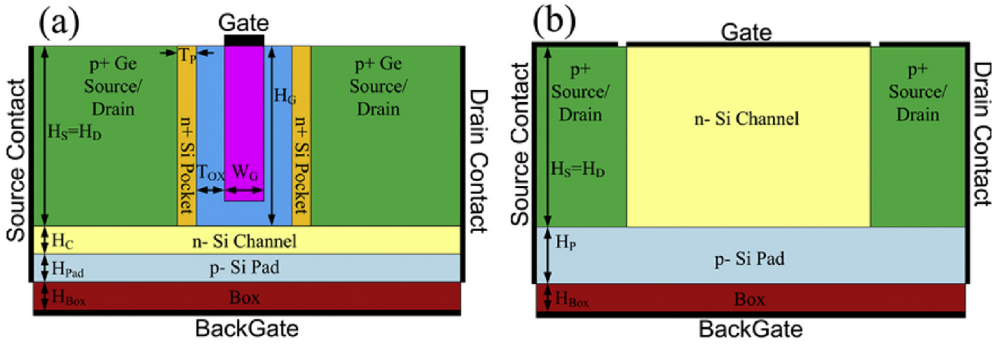

Fig. 1. Schematic of (a) SUTFET and (b) STFET.

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