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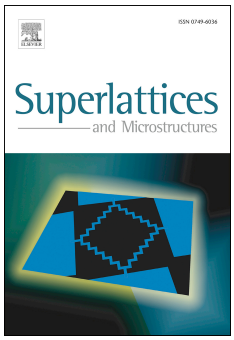

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S. Prasanna Kumar, P. Sandeep, Sudhanshu Choudhary

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Changes in transconductance(g_m) and I_{on}/I_{off} with high-K dielectrics in MX_2 monolayer 10 nm channel double gate n-MOSFET

S.Prasanna kumar[1], P.Sandeep[2] and Sudhanshu Choudhary[3]
School of VLSI Design and Embedded system
[1, 2, 3] National Institute of Technology Kurukshetra-India
E-mail: [1]saragadaprasanna@gmail.com, [2]sandy.payyavula@gmail.com, [3]sudhanshu@nitkkr.ac.in
Phone: +919493929567, +918099165508, +917206550867

***Abstract*: We investigate monolayer Transition Metal Dichalcogenides (TMDs) of type MX_2 (MoS_2, $MoSe_2$, $MoTe_2$, WS_2 and WSe_2) 10 nm n-channel Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) with different dielectrics (SiO_2, Al_2O_3, HfO_2 and TiO_2) using DFT and NEGF formalism. Results suggest that increasing dielectric constant increases both transconductance (g_m) and I_{on}/I_{off} for all type of MX_2 channels. I_{on}/I_{off} and g_m increases by one order with increase in dielectric constant K. Among all type of MX_2 channels considered, WS_2 channels results into highest values of g_m (~ 36.29 uS) and I_{on}/I_{off} ($4.3*10^7$) with TiO_2 dielectric. Variation in Subthreshold Slope (SS) with increase in dielectric constants are negligibly small, SS value of 58.52 mV/dec is obtained with Al_2O_3 dielectric for WS_2 channel. However, a SS value of ~ 60.02 mV/dec is obtained with TiO_2 dielectric for all MX_2 channels. The results suggest that TiO_2 dielectric with WS_2 channel can be used for High Performance (HP) and Low Power (LP) devices since it shows large I_{on}/I_{off} (~ 10^7) and SS around 60 mV/dec.**

***Keywords*— Density functional theory, FET, High-K dielectric, NEGF, Transition Metal Dichalcogenides.**

I. INTRODUCTION

The main motivation behind the reduction in dimensions of MOSFET is to satisfy the demand of low power consumption device in the field of portable electronics such as laptops and mobile phones, as well as to get faster circuits for computational purposes. However, as device dimensions are scaled down, problems which are not present in microscopic level arises, such as quantum confinement of charge carriers which leads to the degradation of device performance. It is evident that the traditional CMOS technology cannot be scaled indefinitely so modifications for traditional CMOS process are needed that is exploring alternative devices such as SET (Single Electron Transistors) or molecular devices. Traditional FETs are based on 3D semiconductor channels which are often composed of silicon and group III-V semiconductors. Over the past five decades, the dimensions of these 3D materials have been successfully scaled down to the nanoscale, plus the introduction of high-k dielectrics have been a successful approach for improving transistor performance [1]. However, reducing the thickness of channel for increasing the gate control is results into a decrease in performance due to the surface roughness scattering, which causes mobility degradation in ultrathin channels [2]. The International Technology Roadmap for Semiconductors (ITRS) 2012 predicts that new type of materials [3] will be needed to address the problems associated with scaling down the geometrical dimensions of transistors in the next 15 years. In past few years, monolayer and multilayer two-dimensional materials have enabled the possibilities of the very thin channel. Graphene has been widely used due to it's remarkable mechanical, thermal and electrical properties. But due to the zero band gap nature of graphene, it's FETs suffer from poor I_{on}/I_{off} and high leakage currents. Therefore, other 2D materials like TMD (Transition Metal Dichalcogenides) of type MX_2, which are having large bandgap opening compared to graphene are explored. TMD material based FETs show better electrostatics compared to Silicon and other group-III and group-V channel based FETs because of their atomic thickness and lower dielectric constant [4].

Different type of simulation approaches have been reported to show the performance limits of TMDFETs at the device level. The first approach uses effective mass based Hamiltonian with ballistic quantum transport simulations using non-equilibrium Green's function (NEGF) formalism. Furthermore, various TMDFETs have been benchmarked for Ultra-scaled devices with attractive switching, gate delay, leakage and energy efficiency [5]. However, to the best of our knowledge, no work has benchmarked Transition Metal Dichalcogenides based FETs with new device options such as using high-k dielectrics in place of SiO_2. Therefore, it is of interest to evaluate and compare these device options with Figure of Merits (FOMs) such as Subthreshold swing (SS), I_{on}/I_{off} and transconductance (g_m).

The high-k dielectric materials play a significant role in the design of novel and high performances devices at the nanoscale level. The high-k materials Al_2O_3 (k~9), HfO_2 (k~25), TiO_2 (k~85) are being actively investigated, for their use as a long-term promising material. These high-k materials are formed by deposition. Many high-k dielectric materials are successfully deposited by Atomic layer deposition. A good gate dielectric should have high dielectric constant, good thermal stability, and large band gap.

In this paper, we investigate TMD based transistors with different channel materials (MoS_2, WS_2, $MoSe_2$, WSe_2, and $MoTe_2$) and for different high-k dielectrics at the device level. Device FOMs such as Subthreshold swing (SS), I_{on}/I_{off} and