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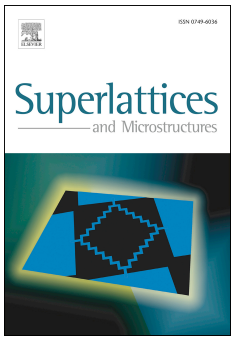

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Study on High Breakdown Voltage GaN-based Vertical Field Effect Transistor with Interfacial Charge Engineering for Power Applications

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ABSTRACT: A high voltage GaN-based vertical field effect transistor with interfacial charge engineering (GaN ICE-VFET) is proposed and its breakdown mechanism is presented. This vertical FET features oxide trenches which show a fixed negative charge at the oxide/GaN interface. In the off-state, firstly, the trench oxide layer acts as a field plate; secondly, the n-GaN buffer layer is inverted along the oxide/GaN interface and thus a vertical hole layer is formed, which acts as a virtual p-pillar and laterally depletes the n-buffer pillar. Both of them modulate electric field distribution in the device and significantly increase the breakdown voltage (BV). Compared with a conventional GaN vertical FET, the BV of GaN ICE-VFET is increased from 1148V to 4153V with the same buffer thickness of 20 μm. Furthermore, the proposed device achieves a great improvement in the tradeoff between BV and on-resistance; and its figure of merit even exceeds the GaN one-dimensional limit.

Keywords: GaN HFETs, Vertical, Heterostructure, Breakdown voltage, Power device

1. Introduction

Gallium nitride (GaN) have attracted a lot of interest for applications in high-power electronics which operate at high temperatures and high frequencies. In the past decades, the advancements of technology make the application prospect of GaN lateral heterostructure field effect transistors (FETs) more and more realistic [1~3]. However, the vertical devices are more desirable than lateral ones because of the superior on-state resistance (R_{on}) [4~6]. Due to the lack of suitable substrates with acceptable defect density ($<10^6$ cm^{-3}) and process complexities, there were challenges for GaN vertical field effect transistors (GaN-VFET) to show their high performance in power electronic fileds during the past years. To solve the substrate problems of GaN-VFETs, *Nie et al.* reported a result of a fabricated outstanding GaN-based vertical transistor in 2014 [7]. Then *Ramya et al.* reported another excellent GaN vertical transistor by utilizing selective area regrowth p-GaN layer in 2015 [8]. These results indicate that high performance homoepitaxial growth on GaN substrates has been realized, and the fabrication technology for GaN vertical transistor has become continuously mature.

Although the fabrication problems have been solved for a certain extent, the reported values of BV for GaN -VFETs are still not so satisfactory. The reported highest average breakdown E-field (150 V/μm) is far below the GaN theoretical limit (340 V/μm) [9]. Indeed the BV of GaN-VFETs is determined by the depletion zone of reverse-biased p-GaN/n-buffer junction [6], and the buffer layers within GaN VFETs are almost not completely depleted, which is an obstacle for increasing the BV of GaN-VFETs. Besides, there is always a serious trade-off between BV and R_{on} for conventional GaN-VFETs. To achieve a higher BV without R_{on}-deterioration, many methods have been carried out. One method is the edge-termination technology which can avoid the premature breakdown; however it does not contribute to expanding the depletion width. Moreover, p-type buried layers and Superjunction structures have been introduced in the buffer layer of GaN-VFETs to achieve high breakdown voltages [9,10]. The p-type buried layers or Superjunction for GaN-VFETs are generally formed by implanting Mg into GaN buffer layers [11].

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