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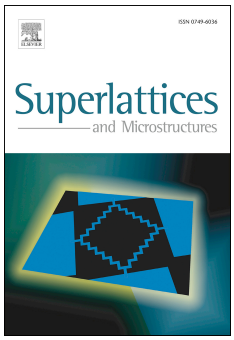

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Investigation of metal-gate work-function variability in FinFET structures and implications for SRAM cell design

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Abstract: In sub-20 nm CMOS technology nodes, the parameter variability has become a main hurdle during the scaling of devices. Recently, the use of metal gate stacks in nano-scale FinFET structure has a significant impact on the intrinsic parameter fluctuations due to the granular nature of metals. A 14 nm FinFET structure has been considered to study the impact of metal-gate work-function variability by using the 3-D device and mixed mode circuit simulation. The present work investigates the impact of work function variability (WFV) on electrical characteristics of various possible FinFET architectures followed by the regression model. Further, the investigation has been extended to study the stability performance of 6-T SRAM cell under the influence of WFV. It is observed that work function variation may result in considerable performance degradation in device as well as SRAM operation in nano domain.

Keywords FinFET, line edge roughness, resist defined, spacer defined, SRAM, work function variation.

1. Introduction

The scaling of planer bulk CMOS technology into future technology generations will face significant challenges due to deprived electrostatic control of gate on channel and increased short-channel effects (SCEs) [1, 2]. Alternative device structures such as ultra-thin body fully depleted silicon-on-insulator (UTB-SOI-MOSFET), double-gate MOSFET, FinFET, gate-all-around FinFET, carbon nano tube FET have been investigated as potential solutions for better gate control and reduced SCEs in nanometer regime [3-6]. Among these non-classical CMOS transistors, FinFET structure has emerged as one of the most promising candidate due to better gate control and fabrication compatibility with conventional CMOS technology [7, 8]. However, in sub-20 nm regime intrinsic process variability sources have posed major problem in FinFET structure. The possible intrinsic process variability sources are random dopant fluctuations (RDF), oxide thickness fluctuations (OTF) and line edge roughness (LER). These have been studied extensively by many authors [9-17]. Moreover, a new source of random fluctuation has been emerged recently through the introduction of metal gate electrodes in advanced CMOS technology. The metal gate electrode has replaced the polysilicon gate in advanced CMOS technology due to elimination of gate depletion effect, enhanced threshold voltage (V_{TH}) control and more importantly it has overcome the high-*k* materials compatibility problem [18-20]. However, metals naturally have a granular structure, where each grain has its own crystal orientation and corresponding work function. Since in sub-nanometer regime the gate dimensions are in range of few tens of nanometer, it is predictable that the gate area contains only a small number of grains. The orientation and work function of each grain is entirely random thus metal gate electrodes suffer from the work function variability (WFV). Recently, for metal gate electrode a mid-gap TiN metal has been extensively used to adjust V_{TH} of the FinFET structure [21-23]. But, because of the combined effect of low number of grain and randomness of their work function, TiN metal gate not only causes variation in V_{TH} but also affects the other performance parameters viz. the on-current variation (I_{ON}), off-current variation (I_{OFF}) and DIBL. Therefore, it becomes extremely necessary to comprehensively analyze the variability introduced by TiN metal gate electrode in FinFET structure and thus in the FinFET based VLSI circuits.

This work thoroughly investigates the device-and circuit variability introduced by TiN metals in resist (i.e. uncorrelated fin LER) and spacer (i.e. correlated fin LER) defined 14 nm FinFET structures using full-scale 3-D device-and mixed mode simulations. A linear regression model has been developed to better understand the statistical behavior of the parameter. To capture the effect of WFV in 14 nm FinFET device, a systematic 3-D "Impedance Field Matching" simulation study has been carried out on large statistical ensembles size.