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A novel trench SOI LDMOS with a dual floating vertical field plate

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ABSTRACT

A novel trench SOI LDMOS with a dual floating vertical field plate structure (DFVFPT SOI) is proposed in this paper. A dual floating vertical plate (DFVFP) is introduced into the filled oxide trench of a conventional trench SOI LDMOS (CT SOI). The DFVFP modulates the distribution of the electric field in the drift region especially the trench surface region, which enhances the internal electric field and effectively prevents premature breakdown, thus increasing the breakdown voltage (BV). At the same time, the doping concentration of the drift region (N_d) is increased because of the assistant depletion effect of DFVFP and a lower specific on-resistance ($R_{on,sp}$) is therefore obtained. Compared with the CT SOI, the $R_{on,sp}$ of the FVFPT SOI can be reduced by more than 35% when its BV can be increased by 27%, and the figure-of-merit (FOM) is enhanced by 145%. Compared with the several structures proposed before, the DFVFPT SOI better improves the tradeoff between BV and $R_{on,sp}$.

1. Introduction

The silicon-on-insulator (SOI) power lateral double-diffused metal-oxide semiconductor (LDMOS) has been widely used in varied fields owing to its inherent advantages of higher reliability, lower power loss and favorable isolation performance [1–3]. Higher breakdown voltage (BV) and lower specific on-resistance ($R_{on,sp}$) are always the aims for the power devices. The trench technologies have been used in the fabrication of power lateral MOSFETs, which makes a shorten cell pitch and leads to a reduced $R_{on,sp}$ [4,5]. On the basis of the trench technology, field plate is integrated in the oxide trench to further reduce $R_{on,sp}$ and enhance the BV [6–9].

In this paper, a novel SOI trench LDMOS (DFVFPT SOI) with dual floating vertical field plate (DFVFP) is proposed. This structure features two FVFPs integrated in the oxide trench, which are exactly symmetrical and form the DFVFP. The assistant depletion effect of the DFVFP leads to a reduced $R_{on,sp}$ and the modulation effect of the DFVFP results in an increased BV for the

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DFVFPT SOI. And therefore, the proposed structure exhibits better performance than the conventional SOI trench LDMOS (CT SOI). The influence of parameters on BV and $R_{on,sp}$ is investigated by semiconductor simulation software MEDICI TCAD [10]. The optimized structure parameter ranges, including those of the plates and oxide trench, are given by a series of analysis, which provides more space of choice for process realization.

2. Device structure and mechanism

Fig. 1(a) shows the device structure schematic cross section of the DFVFPT SOI. The DFVFP integrated in the oxide trench are used to optimize the trench surface field and increase the n-drift doping concentration. W_T and D_T are the width and depth of the oxide trench, respectively. t_s, t_{ox}, t_{sub} and t_p represent the thickness of top-silicon layer, the buried oxide layer (BOX), the p-sub and the field plate respectively. L_{drift} is the length of drift region while *D3* is the length of the field plate. *D1* and *D2* are defined as the vertical and lateral distance between the field plate and oxide trench sides respectively. The specific structure parameters of the DFVFPT SOI are shown in Table 1. In the proposed DFVFPT structure, the plate, oxide and n-drift region compose a metal-insulator-semiconductor (MIS) like structure, which helps to deplete the drift region [11]. Two plates are connected to the gate and drain electrode outside the device working region, respectively. The length and position of the plates can be changed simultaneously which breaks the limitation of conventional VFPs. And DFVFP avoids excessive electrodes extension at the device surface compared with conventional devices with VFP. The space charges distribution under off-state of the DFVFPT structure is shown in Fig. 1(b). At off-state, the gate electrode is connected to the ground while the drain electrode is added a positive voltage. The DFVFP causes different net charges distribution around the trench as shown in Fig. 1(b), which also reflects the concentration difference, leading to reshaping of electric field around the trench sides. Holes and electrons are accumulated at the top and bottom surface of the BOX respectively. Owing to the assistant depletion effect and modulation effect of DFVFP, two new electric peaks come into being and a higher N_d is obtained. The BV of the DFVFPT SOI is therefore increased. And due to the increased N_d, the resistance of the drift region is reduced which leads to a decreased $R_{on,sp}$.

Fig. 2 shows the process realization steps of the DFVFPT SOI: (a) form the trench by etching, before which step the Si_3N_4 layer and SiO_2 layer as hard mask are filled (The SiO_2 layer acts as the buffer to prevents the direct contact of Si_3N_4 and Si which may produce stress and form interface state) [12]; (b) fill the trench by thermal oxidation; (c) etching of oxide and deposition of DFVFP which calls for much accurate control with depositing velocity due to the exact height required [13,14]; (d) fill the trench by thermal oxidation followed by ion implantation for forming the n+, p+ and p-well regions (The reason why ion implantation procedure stands after oxide trench fabrication is that high temperature generated by etching and deposition process may cause secondary diffusion of impurities which needs to be avoided as far as possible); (e) electrode formation. The technological challenges in realizing such a structure mainly consist of the accurate deposition of DFVFP, the extension and connection between plates and electrodes. The former one calls for special masks which are used to deposit symmetrical plates, and the latter one is conducted outside working region of the device.

3. Results and discussion

3.1. Static characteristics analysis

Fig. 3 shows the 3D electric field distributions around the oxide trench region of two structures, in which the dashed area represents the inner space of oxide trench. Fig. 3(a) is the electric field distribution of the CT SOI, in which there is electric field peak at the drain side (D in Fig. 1(a)) and reaches to the silicon critical field prematurely. It is clear in Fig. 3(b) that the electric field on the interface of silicon and the oxide trench is reshaped after the introduction of DFVFP. The DFVFPT SOI introduces a high electric field from the surface of the device to the bulk, especially the region around two plates. The DFVFP increases the overall internal electric field, meaning the voltage endurance capability of oxide trench is enhanced, which effectively avoids premature breakdown of device. Fig. 4 is given below to better figure out the specific electric field distributions.

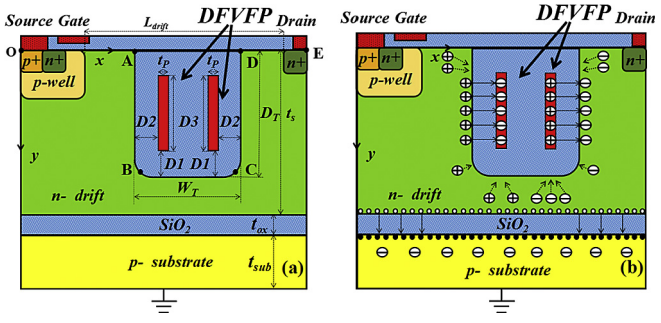

Fig. 1. Schematic cross section of DFVFPT SOI LDMOS. (a) Device structure. (b) Space charges distribution at off-state.

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