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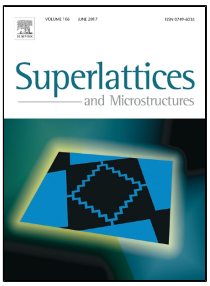

Impact of Channel Thickness and Spacer Length on Logic Performance of p-Ge/n-Si Hybrid CMOSFETs for ULSI Applications

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Highlights

- Logic performance of HCMOSFET comprising p-Ge & n-Si MOS devices is reported.
- Effects of channel thickness and spacer length on HCMOSFET parameters are studied.
- Rise time for HCMOS inverters reduce significantly compared to Si inverters.
- HCMOS based ring oscillator exhibits much higher frequency of oscillations.
- HCMOSFET outperforms its Si counterpart for logic circuit applications.