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Novel tri-independent-gate FinFET for multi-current modes control

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ABSTRACT

In this paper, a novel tri-independent-gate (TIG) FinFET is presented for multi-current modes control for the first time. The entire integration flow of proposed TIG FinFET is fully compatible with the mainstream gate-first HKMG FinFET process. Five kinds of ON state modes and threshold voltages can be offered by TIG FinFET without additional voltage sources, and it is demonstrated to have a great potential in dynamic voltage SRAM design. The critical electrical parameters of TIG FinFET in different modes are fully investigated with TCAD simulation and compared to the traditional FinFET. TIG FinFET with double fins is found to possess a distinct different output and capacitance characteristics with single fin FinFET. The underlying physical mechanisms are analyzed and investigated in detail.

1. Introduction

As the traditional bulk MOSFET continuous scaling down, the reduced gate control ability results in severe short-channel effects (SCEs), which brings problems such as threshold voltage roll-off, subthreshold swing deterioration and leakage current increment. FinFET has become one of the mainstream devices over the past few years to overcome SCEs [1–3]. However, due to the quasi-planar structure, the width of FinFET only can be increased in quanta of fin height [4]. The width quantization brings much inconvenience in FinFET-based circuit design, especially in static random access memory (SRAM), which has self-conflicting design requirements and need appropriate transistor sizing for cell stability [5].

In order to increase the transistor flexibility, double-independent-gate (DIG) FinFET has been proposed [6–8] and gained great attention in SRAM design [9,10]. In DIG FinFET, the front gate works as drive gate while the back gate works as V_{th}-control gate, and then a flexible threshold voltage is obtained as the back gate voltage varies. However, one should bear in mind that in order to get various threshold voltages in DIG FinFET, an additional voltage source is needed to control the back gate, which will inevitably increase the complexity of circuit design. Otherwise, only two different threshold voltages and current modes can be offered: single-gate mode and dual-gate mode. Moreover, the current of single-gate mode is less than forty percent of dual-gate mode [9], which will bring significant increment in circuit delay. For instance, once the single-gate mode DIG FinFETs are used in SRAM to enhance the read stability, it will inevitably bring severe read delay penalty.

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In this paper, we present a novel tri-independent-gate (TIG) FinFET. Besides a modified HKMG process, the fabrication flow for TIG FinFET is fully compatible with the mainstream gate-first HKMG FinFET process. The proposed TIG FinFET has three independent gates: top gate, bottom gate1 and bottom gate2. Because of the symmetry of bottom gate1 and bottom gate2, five kinds of threshold voltages and current modes can be offered in TIG FinFET with single voltage source, which brings more flexibility than DIG FinFET. In addition, the threshold voltages in TIG FinFET are able to be changed without significant delay penalty, which can be applied to SRAM design to get appropriate tradeoff between read stability and speed. The fabrication flow for TIG FinFET is proposed in Section 2. Section 3 deeply investigates the current characteristics of TIG FinFET with single fin and double fins, and the effect of additional fringe capacitance in TIG FinFET is also discussed in this part. The conclusion is given in Section 4.

2. Fabrication flow for tri-independent-gate (TIG) FinFET

Fig. 1 (a) shows the structure of proposed single fin TIG FinFET with three independent gates: top gate, bottom gate1 and bottom gate2. The structure fabrication of TIG FinFET is fully compatible with the mainstream gate-first HKMG FinFET process, besides a modified five-step HKMG process, as the red parts depicted in Fig. 1 (b). After STI formation processing finished, the gate oxide layer with thickness higher than fin height is deposited, and then the first additional CMP processing is performed to remove the gate oxide above the top of fin. Next, the extra part of gate oxide is etched back, only remaining the required part on the two sides of fin. Afterwards, the gate metal layer is deposited and the second additional CMP processing is performed to make sure the gate metal layer has the same height as gate oxide and fin. The key issue for the two additional CMP processing is to stop CMP at the appropriate location to ensure the fin height remains constant. After the second additional CMP processing, two independent bottom gates are formed. Finally, the gate oxide layer and gate metal layer are respectively deposited to form the top gate. The above process flows are shown in Fig. 1 (c), which form the modified HKMG process. It is worth noting that the top gate oxide layer and bottom gate oxide layer are formed separately, hence, the dielectric layers with different types and thickness can be chosen for top and bottom gate oxide to optimize the device

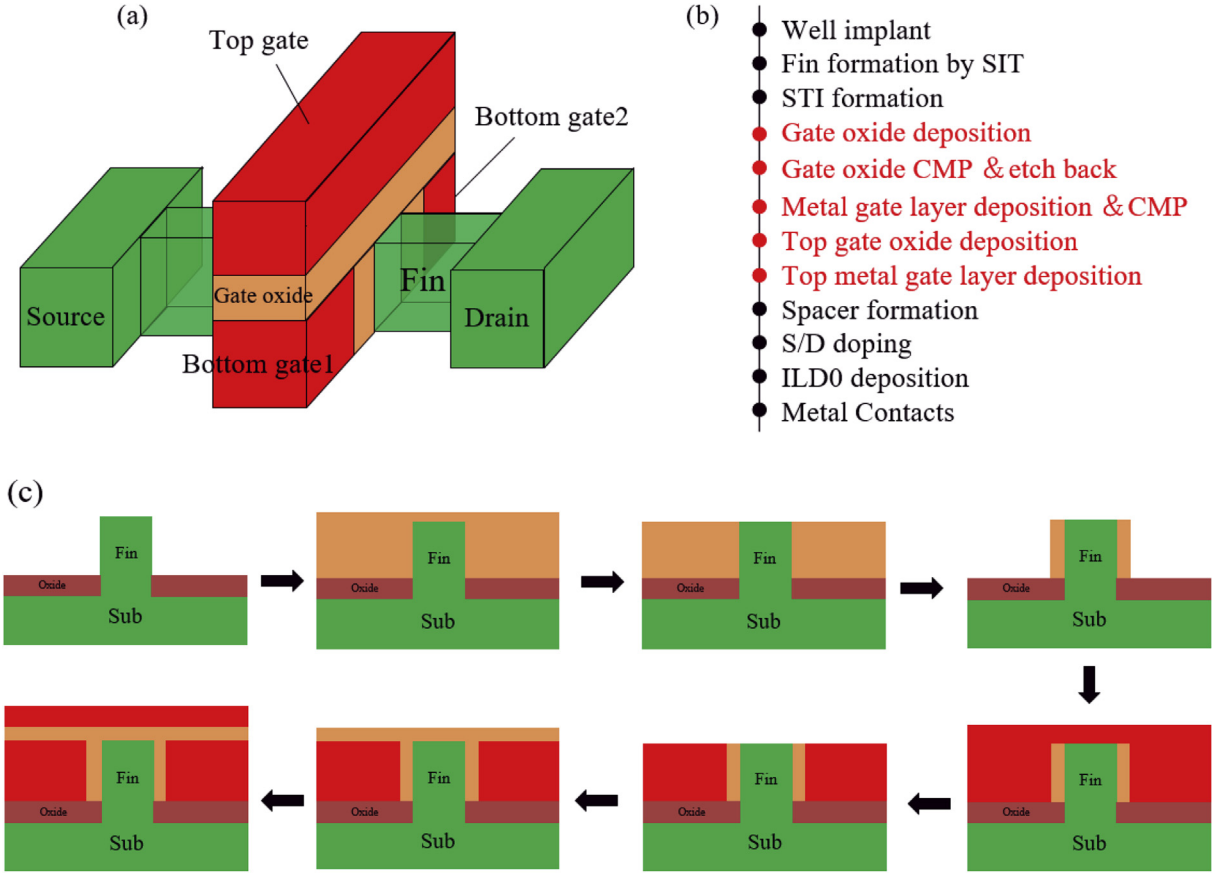

Fig. 1. Structure and fabrication flow for single fin TIG FinFET. (a) Single fin structure for TIG FinFET. (b) Process flow for single fin TIG FinFET and (c) fabrication flow for modified HKMG process in single fin TIG FinFET.

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