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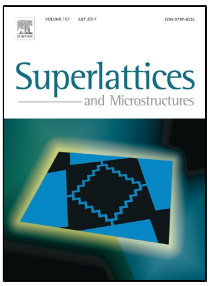

Effect of Trench Depth and Gate Length Shrinking Assessment on the Analog and Linearity Performance of TGRC-MOSFET

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Effect of Trench Depth and Gate Length Shrinking Assessment on the Analog and Linearity Performance of TGRC-MOSFET

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***Abstract*--**This paper discusses the impact of trench depth (Negative Junction Depth (NJD)) and gate length (L_G) shrinking on analog and linearity performance of Transparent Gate Recessed Channel (TGRC) MOSFET with an aim to achieve a reliable and high performance transistor. It is found that device enhances the I_{ON} by 38% and thereby improves the analog performance in terms of transconductance, device efficiency, output resistance, and gain. Moreover, linearity figure of merits are also enhanced at lower gate bias in TGRC MOSFET in comparison to conventional and Conventional Recessed Channel (CRC) MOSFET due to reduced harmonic distortions (g_{m3}). Thus, the improved analog and linearity performance at 5 nm NJD and 20 nm L_G of TGRC-MOSFET makes it suitable for low power linear RF amplifiers as a nano-scaled device. Thus, these results would serve as a worthy design tool for low power and high performance CMOS circuits.

***Keywords*—**Analog, Distortions, Linearity, TGRC-MOSFET, Trench gate, Transconductance coefficients.

1. Introduction

For RFIC designing and high-frequency applications, CMOS devices are required with low intermodulation distortion to sustain linear operations when working with a weak signal. In modern communication systems, a high linearity is desired so as to exhibit less distortion. Intermodulation (IM) may induce when the system gives nonlinearity performance and generate different frequency signal at outputs compared to input signal frequency. This kind of interference may fall into the band of interest and distorted the desired output [1]. However, sub-nm MOSFET exhibit linear relation but short channel effects (SCEs) hinders its linearity. As the dimensions of the device are reduced, scaling the silicon-based MOSFET devices for barrier potential, critical electric field, oxide thickness, threshold voltage, etc., are becoming hardly increased [2]. To overwhelmed such scaling problems, various device engineering schemes (gate, channel and drain engineering, etc.) and numerous device structures such as multi-gate MOSFET by Barsan in 1981 [3], SOI MOSFET by An et al. in 2003 [4], Conventional Recessed Channel (CRC) MOSFET by Chaujar et al. in 2008 [5], GAA MOSFET by Auth et al. in 1997 [6], and Silicon Nanowire MOSFET by Gupta et al. in