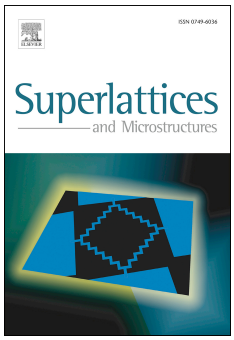
Accepted Manuscript



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PII: S0749-6036(17)30832-7

DOI: 10.1016/j.spmi.2017.04.015

Reference: YSPMI 4942

To appear in: *Superlattices and Microstructures*

Received Date: 5 April 2017

Accepted Date: 8 April 2017

Please cite this article as: S.P. Scarlet, R. Ambika, R. Srinivasan, Effect of eccentricity on junction and junctionless based silicon nanowire and silicon nanotube FETs, *Superlattices and Microstructures* (2017), doi: 10.1016/j.spmi.2017.04.015.

Effect of Eccentricity on Junction and Junctionless based Silicon nanowire and Silicon nanotube FETs

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***Abstract*— In this paper, the effect of eccentricity on Junction-based Silicon Nanowire FET, Junction-based Silicon Nanotube FET, Junctionless-based Silicon Nanowire FET, and Junctionless-based Silicon Nanotube FET is investigated. Three kinds of eccentric structures are considered here. The impact of eccentricity on effective gate oxide thickness thereby gate oxide capacitance, and effective channel width are studied using 3D numerical simulations. Average radius of an ellipse is used to generate a model which captures the impact of eccentricity on gate oxide capacitance, and verified using TCAD simulations in MOS nanowire structure. The impact of eccentricity on ON current (I_{ON}), OFF current (I_{OFF}), I_{ON}/I_{OFF} ratio, and Unity gain cutoff frequency are investigated. Eccentricity increases the effective gate oxide thickness, the effective channel width, I_{ON}, and I_{OFF} but reduces I_{ON}/I_{OFF} ratio.**

Keywords—Silicon nanowire, Silicon nanotube, eccentricity, junctionless

I. INTRODUCTION

Short channel effects (SCE) associated with the conventional-bulk-planar MOSFET scaling are forcing us to investigate multigate structures (FinFETs, Trigate-FET, quadruple gate and Gate All Around) and other novel devices (junctionless devices, tunneling devices etc). Among multigate structures, Gate All Around (GAA) devices, also known as nanowires, provide better SCE performance [1]-[3]. Nanowires can be fabricated having square or circular cross section [4]. The circular nanowires enjoy the benefit of multigate structures along with the lower effective gate oxide thickness which is beneficial for better gate control without compromising gate oxide tunneling. Even though the physical oxide thickness (T_{OX}) of a parallel plate capacitor and cylindrical capacitor (with circular cross section) are same the cylindrical capacitor undergoes a reduction in T_{OX} which can be captured by the effective gate oxide thickness (T_{OX_EFF})[5]. Silicon nanotube FETs (SiNT-FET) are the latest version of multigate structures [6]. Since tube has two surfaces, one inside and another outside, two gates control the channel and thus offer superior performance over nanowires. Both nanowires and nanotubes are investigated on junction and junctionless devices [7],[8]. Junctionless device which is devoid of junctions due to uniform doping in source, channel and drain regions is also popular to reduce the SCE [9]-[12].

Apart from the SCE, process variations are also one of the important parameters in nano regime. The impact of process variations in nanowire junction-based FETs is investigated in the literature [13] and similarly nanowire junctionless devices [14] are studied for process variations. Since the SiNTs are comparatively newer devices the impact of various structural and doping parameters are yet to be investigated and understood. Eccentricity is a common process variational problem for nanowires and nanotubes. Circular cross sectioned structures undergo an elliptical change due to process variations. In case of elliptical cylinders, the eccentricity affects the T_{OX_EFF} and the effective channel width (W_{EFF}) which is nothing but the perimeter of the cylindrical structures. This in turn changes the gate oxide capacitance (C_{OX} given per unit area). The impact of eccentricity on gate capacitance (with confocal ellipses) of nanowires is analyzed in [15] but the impact of eccentricity on basic device parameters, I_{ON} and I_{OFF}, is yet to be studied. Since SiNT-FET is a recent structure the effect of eccentricity on these structures is yet to be investigated.

It would be interesting to have a study which focuses on the basic device characteristics of the nanowires and nanotubes from the eccentricity point of view. In this work, the effect of eccentricity is studied on the following devices.

(i) Junction-based Silicon Nanowire FET (SiNW-FET)
(ii) Junction-based Silicon Nanotube FET (SiNT-FET)
(iii)Junctionless-based Silicon Nanowire FET (JLSiNW-FET)
(iv)Junctionless-based Silicon Nanotube FET (JLSiNT-FET)

As can be seen from the above list, both junction and junctionless devices are studied. A simple model is proposed for T_{OX_EFF} and C_{OX}, for three different cases, namely (i) common eccentricity (ii) concentric (iii) confocal ellipses. The impact of eccentricity on I_{ON} and I_{OFF} is also studied through numerical simulations, for devices listed above. Basic RF parameter, f_T is also looked in from the eccentricity point of view.

Rest of the paper is organized as follows: Next section discusses about the device structures and their I_D-V_G calibrations. In section 3, a cylindrical MOS structure is studied for eccentricity. The effect of eccentricity in SiNW-FET, JLSiNW-FET, SiNT-FET and JLSiNT-FET are discussed in Section 5. Finally the conclusions are provided in section 6.

II. DEVICE STRUCTURE AND I_D-V_G CALIBRATION

TCAD simulator is used for simulations. Sentaurus structure editor (SDE) is used to create the device structure and to generate mesh for device simulation. Sentaurus device (SDEVICE) is used to perform the DC, AC device simulations. Drift-diffusion