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Effect of FIBL in-conjunction with channel parameters on analog and RF FOM of FinFET

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ABSTRACT

In this paper, the effect of fringe induced barrier lowering (FIBL) in-conjunction with channel parameters that includes channel thickness (T_{Si}), channel length (L_g) and lateral straggle (σ_L) on analog and RF performance of FinFET, have been studied using TCAD mixed-mode Sentaurus device simulator. We focused on the variation in analog (intrinsic dc gain) and RF (cut-off frequency) figure of merit (FOM) of high-*K* gate dielectric based FinFET with respect to channel parameters. It is observed that the variation in intrinsic dc gain (ΔA_V) aggravates with T_{Si} scaling. We also observe a mixed response to the ΔA_V with respect to variation in L_g and σ_L, where ΔA_V follows an inverse parabolic behavior peaking at an intermediate value of L_g and σ_L. Variation in cut-off frequency (Δf_T) on the other hand, is negligible (slightly increases with T_{Si} and decreases with L_g and σ_L). These properties of channel parameters can be handy in designing of high-*K* gate dielectric based FinFET for analog circuits.

1. Introduction

LOW power consumption and high frequency of operations are the main challenges faced by the high density integrated circuits these days. The complicacy in CMOS design has been introduced by scaling geometric dimensions of the MOSFET. One of the limitation in scaling of CMOS devices is the increase in gate tunneling current attributed to lower gate dielectric thickness [1,2]. CMOS with gate length below 100 nm will need an oxide thickness of less than 1.5 nm. Such a thin oxide layer result in high direct tunneling gate leakage current [3] and thus it will increase the static power dissipation resulting in limited device performance. To get rid of this critical problem, high-*K* dielectrics have been introduced by directly depositing them on the silicon wafer, while keeping the equivalent oxide thickness (EOT) constant. Subsequently, the physical thickness of gate dielectric can be increased by a factor of *K*/3.9 resulting in much lesser direct gate tunneling current [4–6]. A much thicker physical gate dielectric layer however, leads to reduced gate coupling, which deteriorate the gate control over the channel and compromise the short-channel performance [7,8]. Mohapatra et al. [9–11] presented the detailed analysis of fringe induced barrier lowering (FIBL) on digital performance of MOS transistors with high-*K* gate dielectric. They suggested that due to reduced gate coupling, the drain control on the source to channel barrier height is increased substantially.

FIBL effect can also be illustrated with the help of energy band diagram along the channel [12]. Fei et al. [13] describes the influence of FIBL effect in terms of equivalent coupling capacitance (C_{CP}) using different device attributes such as gate length,

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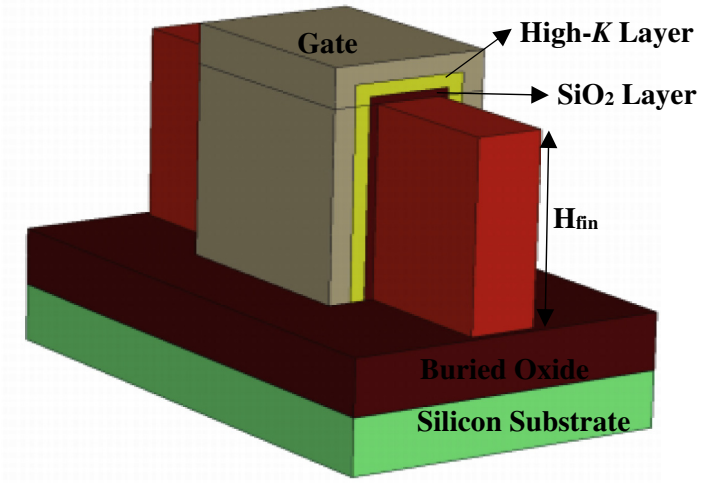
junction depth and spacer permittivity. They show that with the decrease in channel length or increase in junction depth, C_{CP} increases and hence threshold voltage decreases in a single gate MOSFET. Substantially, the intrinsic dc gain (A_v) decreases with decrease in threshold voltage (V_{th}) [14]. Few recent research has also been conducted to understand the effect of high-*K* dielectrics on analog and RF performance of the DG-MOSFET. Nandi et al. [15] shows that intrinsic dc gain decreases with high-*K* gate dielectric in an underlap DG-MOSFET. Pradhan et al. [16], presented that, the high-*K* gate dielectric with gate stack are best suited for analog and RF performance of DG-MOSFETs.

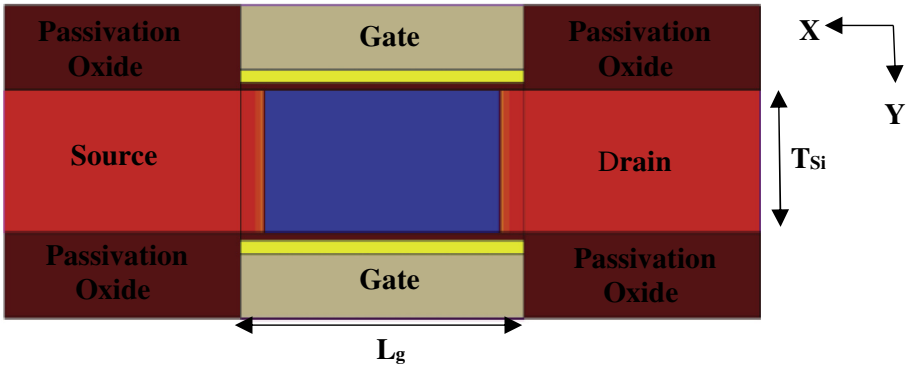
In the present work, extended simulations have been performed on the TCAD mixed mode simulator to study the effect of high-*K* gate dielectrics in-conjunction with channel parameters of FinFET devices. By considering different channel parameters, we have studied the impact of high-*K* gate dielectric on the analog and RF performance of the device. The rest of this paper is organized as follows: Section 2 presents the device structure and simulation framework used. Device physics is explained in section 3. An analysis of the effect of high-*K* gate dielectrics on Analog FOM (such as output conductance (g_{ds}), transconductance (g_m), A_V and ΔA_V) and RF FOM (such as f_T and Δf_T) of FinFET under different channel parameter is carried out in Section 4 and finally the conclusion is drawn in section 5.

2. Device structure and simulation framework

Fig. 1 shows a 3-D symmetric FinFET structure and its 2-D view along X-Y plane. The drain and source extensions are 35 nm long from the gate edges and are heavily doped as n-type with doping concentration = 10^{20} cm^{-3} to reduce the effect of mobility degradation by coulomb scattering [16]. The channel is doped as p-type with doping concentration $N_C = 10^{16}$ cm^{-3}. The SiO_2/high-*K* stacked gate-oxide structure having SiO_2 thickness = 0.2 nm has been preferred over the structure of high-*K* dielectric placed directly on the silicon channel to avoid the adverse effect of interface defects at the high-*K*/Si-channel



(a)



(b)

Fig. 1. (a) 3-D schematic of FinFET (b) 2-D view along X-Y plane.