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A novel nanoscaled Schottky barrier based transmission gate and its digital circuit applications

Sunil Kumar [a], Sajad A. Loan [a, *], Abdulrahman M. Alamoud [b]

[a] Department of Electronics and Communication Engineering, Jamia Millia Islamia, New Delhi, India
[b] Department of Electrical Engineering, King Saud University, Saudi Arabia

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ABSTRACT

In this work we propose and simulate a compact nanoscaled transmission gate (TG) employing a single Schottky barrier based transistor in the transmission path and a single transistor based Sajad-Sunil-Schottky (SSS) device as an inverter. Therefore, just two transistors are employed to realize a complete transmission gate which normally consumes four transistors in the conventional technology. The transistors used to realize the transmission path and the SSS inverter in the proposed TG are the double gate Schottky barrier devices, employing stacks of two metal silicides, platinum silicide (PtSi) and erbium silicide (ErSi). It has been observed that the realization of the TG gate by the proposed technology has resulted into a compact structure, with reduced component count, junctions, interconnections and regions in comparison to the conventional technology. The further focus of this work is on the application part of the proposed technology. So for the first time, the proposed technology has been used to realize various combinational circuits, like a two input AND gate, a 2:1 multiplexer and a two input XOR circuits. It has been observed that the transistor count has got reduced by half in a TG, two input AND gate, 2:1 multiplexer and in a two input XOR gate. Therefore, a significant reduction in transistor count and area requirement can be achieved by using the proposed technology. The proposed technology can be also used to perform the compact realization of other combinational and sequential circuitry in future.

1. Introduction

The driving force for the integrated circuit technology growth is the scaling of metal oxide semiconductor field effect transistor (MOSFET) device dimensions. It is scaling predominantly that has kept Moore's law valid till date and is responsible for the performance enhance in the integrated circuits. The increase in speed, packing density, functionality etc can be attributed to the scaling of device dimensions only [1–3]. However, the scaling of technology node below 18 nm is cumbersome, as various short channel effects (SCE) in the MOS devices prevent the scaling further and further, significantly degrade the device performance and severe reliability issues arise [4,5]. The gate tunneling, leakage power, series resistance associated with the source and drain regions increases significantly in a nanoscaled device [6,7]. The source/drain (S/D) series resistance (R_{SD}) is a serious issue faced by devices with nanoscaled dimensions. The International Technological Roadmap for

* Corresponding author.
E-mail addresses: sloan@jmi.ac.in, sajadiitk@gmail.com (S.A. Loan).

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semiconductors (ITRS) has predicted that (R_{SD}) is a serious issue and apparently there is no potential solution for this issue [8]. The use of raised S/D regions has mitigated this problem to some extent; however, it has swelled the gate to S/D ($C_{G\text{-}S/D}$)) capacitances and has complicated the fabrication process. A potential solution to the S/D series resistance is to use the metal or metal silicide source/drain (S/D) regions instead of the conventional doped S/D regions. A significant reduction in S/D series resistance and a reduced thermal budget is achieved by using metal S/D regions in nanoscaled MOS devices [9,10,20–23]. Further, since scaling below 18 nm is extremely difficult in silicon devices, it is the need of hour to replace silicon with some other materials, like wide bandgap materials, or to go for the structural changes in silicon based devices. A potential approach is to realize multifunctional devices which can directly realize a circuit action [11,12].

In our previous work, we developed some multifunctional devices [13–15]. A single transistor double gate Schottky MOSFET, called as Sajad-Sunil-Schottky (SSS) [13] has been designed and simulation. The SSS device successfully realizes *n* and *p* type MOS actions and realizes a complete inverter action. The SSS device has been modified further and a new double gate Schottky MOSFET has been designed and simulated. This device can easily replace the NMOS/PMOS parallel combination in a conventional TG. The proposed transmission path transistor [14,15] has less number of junctions, regions, interconnections and is highly compact in comparison to the conventional TG. This work focuses on the design of a compact and highly scalable transmission gate employing the proposed transmission path transistor and the SSS device. A transmission gate (TG) is an important digital circuit and has a vast application domain. In addition to transmitting the data from the input to output without signal degradation; it can realize various combinational circuits. Therefore, improving the performance of a transmission gate will get reflected in improving the performance of the various combinational circuits it can realize, like adders, multiplexers, XOR gates, flip-flops, SRAM *etc* [16,17,25]. However, the requirement of four transistors in a conventional TG is a big problem in comparison to a simple pass transistor, which consumes just one transistor [18,19].

In our earlier work [14,15], we performed the simulation study of a single transmission path double gate Schottky MOSFET, which has been used as a transmission path transistor in a transmission gate. We have directly used Φ and $\overline{\Phi}$, the two complementary gate signals, driving the top and bottom gates of the transmission path transistor. In this extended work, we initially design and simulate a complete combined transmission gate, employing the transmission path transistor developed in Ref. [15] and the SSS inverter [13]. The two complementary gate signals have not been used directly; however, they have been realized by using the SSS inverter. The use of the proposed double gate transmission path transistor along with the SSS inverter device in the proposed TG has resulted in a substantial reduction in interconnections, junctions, regions and components and is responsible for the compactness of the proposed transmission gate.

Further, an important work done in this paper is the development of various applications of our SSS device and the transmission path transistor. The proposed transmission path transistor along with the SSS device has been used to realize some combination circuits, like a two input AND gate, 2:1 multiplexer and an XOR gate It has been observed that the transistor count has halved in realizing the AND gate, multiplexer and the XOR gate using the proposed technology, for the first time. All these circuits are realized by using the three transistors only unlike the use of six transistors in the conventional technology. The proposed technology can be also used to perform the compact realization of other combinational and sequential circuits.

The paper is divided into five sections. Section 2 describes the proposed device structures. The simulation setup and the operational mechanism of the proposed TG is discussed in Section 3. Section 4 describes the realization of various circuits using the proposed technology. The paper is concluded in Section 5.

2. Device stuctures

Fig. 1 shows the schematic diagram of the full transmission gate employing our double gate Schottky transistor [14,15] for the transmission path and our SSS inverter [13] for realizing the complementary gate signals for the transmission path transistor. In the transmission path transistor, the top and bottom gates work functions are 4.45eV and 4.95eV respectively. The work functions are chosen to have optimum *n* and *p* mode operations in the transmission path transistor. The proposed transmission path does not employ doped source and drain regions, however, two metal silicides, Erbium silicide and

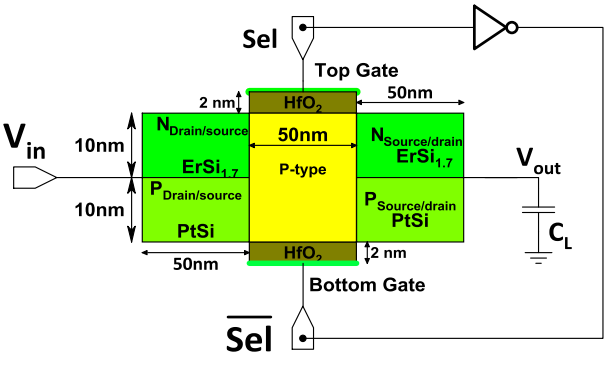

Fig. 1. Schematic diagram of the proposed transmission gate, transmission path transistor.