Superlattices and Microstructures 104 (2017) 470–476

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Investigation of 6T SRAM memory circuit using high-k dielectrics based nano scale junctionless transistor

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ARTICLE INFO

Article history:
Received 24 February 2017
Accepted 6 March 2017
Available online 8 March 2017

Keywords:
High-k
SRAM
Junctionless transistor
Dual metal gate engineering
TCAD

ABSTRACT

In this paper the Dual Metal Surround Gate Junctionless Transistor (DMSGJLT) has been implemented with various high-k dielectric. The leakage current in the device is analysed in detail by obtaining the band structure for different high-k dielectric material. It is noticed that with increasing dielectric constant the device provides more resistance for the direct tunnelling of electron in off state. The gate oxide capacitance also shows 0.1 μF improvement with Hafnium Oxide (HfO_2) than Silicon Oxide (SiO_2). This paved the way for a better memory application when high-k dielectric is used. The Six Transistor (6T) Static Random Access Memory (SRAM) circuit implemented shows 41.4% improvement in read noise margin for HfO_2 than SiO_2. It also shows 37.49% improvement in write noise margin and 30.16% improvement in hold noise margin for HfO_2 than SiO_2.

1. Introduction

The semiconductor industry performs intensive scaling in the recent years which results in tiny gate dimension of 14 nm technology node. Due to this scaling, the fabrication process becomes much complicated due to the concentration gradient to be obtained for the device from source to drain. The distinct junction in the tiny dimension needs expensive fabrication technique. Thus device without junction will be a better alternative to extinguish this bottleneck [1]. The device switching is provided by the difference in work function between gate metal and silicon region. This device also shows improved performance than the inversion mode device in terms of leakage current, subthreshold slope and DIBL [1,2]. Many works on junctionless transistor have been published recently stating the improvements in the device parameters [3–9].

Though the device shows improved performance, the short channel effects and leakage current is found to be a problem. The cylindrical structure controls the short channel effects to a grater extend [10]. The dual metal gate engineering techniques improve carrier transport efficiency and drain current in the device [11–13]. The dual metal gate engineering in cylindrical structure has been implemented and found to have short channel and carrier transport performance [14,15].

In this work different high-k dielectrics based DMSGJLT is implemented. The energy band diagram of the device is obtained and with this, the leakage characteristic is analysed in the subthreshold region. The path of tunnelling is taken for the device with both SiO_2 and HfO_2 gate dielectrics. The tunnelling path is large with HfO_2 in the subthreshold state when compared with SiO_2 in the drain region. The energy gap between conduction band and fermi level is higher in case of HfO_2. Due to this, the high-k dielectrics also deliver a low band to band leakage current. The capacitance of the device shoots up

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http://dx.doi.org/10.1016/j.spmi.2017.03.012
0749-6036/

with increasing dielectric constant, hence the charge holding capability of HfO_2 based DMSGJLT is high due to large capacitance value of the device. Thus leakage of charge carriers decreases and DMSGJLT with HfO_2 gate dielectrics elevate the memory performance when implemented in 6T SRAM. Thereby high-k dielectric based DMSGJLT delivers less leakage of charge carriers and in brief can be used for memory application such as 6T SRAM.

2. Device structure

The device structure of the DMSGJLT is shown in Fig. 1. This is a dual metal gate engineered structure with first gate of workfunction 4.97 eV and second gate of workfunction 4.27 eV as taken from Ref. [14,16]. Both the gates are taken as equal length with $L_1 = L_2 = 20$ nm. The centre silicon rod has a doping concentration of 2×10^{19} cm^{-3} uniform in the full stretch of the device from source to drain.

Due to the high band gap of 9 eV of SiO_2, it has been used as gate oxide for many years. The frequent scaling of the device decreases the oxide thickness to 2 nm. Due to this tunnelling leakage, current increases and elevates power consumption [16–19].

The sentaurus TCAD tool is used for simulation, and it employs the physical model such as temperature dependent carrier transport model, band gap narrowing model and quantum models. Radiative recombination, Auger and Shockley-Read-Hall (SRH) are also included for leakage current analysis.

2.1. Results and discussion

The OFF state band diagram of SiO_2 and HfO_2 based DMSGJLT is shown in Fig. 2. This type of band analysis is made in Ref. [20,21]. The high-k gate dielectric such as HfO_2 offers high resistance in the OFF state to the device. Consequently, it is observed that HfO_2 dielectrics based device has a higher conduction band energy level than SiO_2 dielectrics based device. Table 1 shows the properties of different material which is used as gate dielectrics for this analysis.

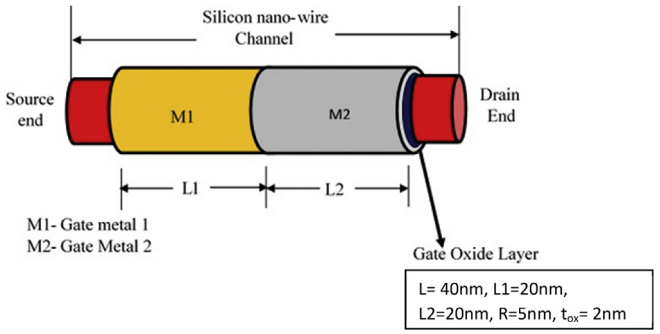

Fig. 1. 3D view of DMSGJLT.

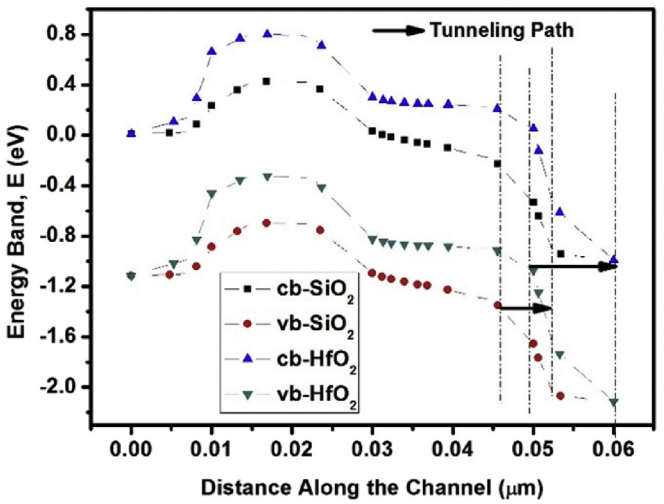

Fig. 2. OFF State Channel Region Energy Band for the Device with SiO_2 and HfO_2 gate Dielectrics.