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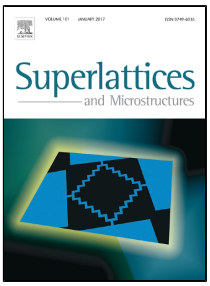

Line edge roughness induced threshold voltage variability in nano-scale FinFETs

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- Threshold voltage performance of FinFET due to varies LER (resist defined and spacer defined) which can be present during the fin pattering process has been performed with isolation and in presence of other statistical variabilities i.e. RDF, OTV and WFV.

- Among all the statistical variabilities apart from LER, the oxide thickness variation and work function variations are dominating the threshold voltage.

- Our finding suggest that spacer defined FinFET structures are more immune to LER variabilities due to correlated LER.