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Improving breakdown voltage and self-heating effect for SiC LDMOS with double L-shaped buried oxide layers

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ABSTRACT

In this paper, a SiC LDMOS with double L-shaped buried oxide layers (DL-SiC LDMOS) is investigated and simulated. The DL-SiC LDMOS consists of two L-shaped buried oxide layers and two SiC windows. Using 2-D numerical simulation software, Atlas, Silvaco TCAD, the breakdown voltage, and the self-heating effect are discussed. The double-L shaped buried oxide layers and SiC windows in the active area can introduce an additional electric field peak and make the electric field distribution more uniform in the drift region. In addition, the SiC windows, which connect the active area to the substrate, can facilitate heat dissipation and reduce the maximum lattice temperature of the device. Compared with the BODS structure, the DL-SiC LDMOS and BODS structures have the same device parameters, except of the buried oxide layers. The simulation results of DL-SiC LDMOS exhibits outstanding characteristics including an increase of the breakdown voltage by 32.6% to 1220 V, and a low maximum lattice temperature (535 K) at room temperature.

1. Introduction

Silicon carbide (SiC) has been widely used to make high-temperature, high-voltage and high-power devices because of its inherent material qualities, such as wide bandgap (3–3.2 eV), high critical field (2.5–3 MV/cm) and large thermal conductivity (4–5 W/cm-K) [1,2]. Because of its excellent properties, SiC has more advantages in large power applications than Si [3]. Among the different SiC polytypes, 4H-SiC is regarded as the most suitable material due to its high and isotropic bulk mobility [4]. Several groups have successfully attempted to improve SiC vertical power MOSFETs [5]. Compared to vertical power MOSFETs, SiC lateral double-diffusion metal oxide semiconductor (LDMOS) devices are more suitable for power integrated circuits (IC) because all ports are on the same surface and it is ease to combine low voltage CMOS signal-processing circuits with high-voltage LDMOS drivers on the same chip [6–9].

On the other hand, lateral power MOSFETs on silicon-on-insulator (SOI) substrates have been intensely studied by many researchers because of their ideal dielectric isolation [10,11]. However, buried oxide layers can prevent the vertical electric field extension and the heat dissipation, which cause SOI LDMOSFETs to suffer from low breakdown voltages and self-heating effects. In order to improve the breakdown voltage, different techniques have been used in SOI LDMOS. These include the reduced surface field (RESURF) principle [12–15], patterned buried oxide layers, fixed charges [16–18], and the enhanced dielectric field (ENDIF) effect [19,20]. Furthermore, an effective way to solve the problem of self-heating effects is the partial

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SOI (PSOI) technique. PSOI works because there is a Si window under the source and channel region which can prevent the bad influence of the poor thermal conduction of buried oxide layers [9,10,21,22].

In this paper, we study and simulate a SiC LDMOS with double L-shaped partial buried oxide layers (DL-SiC LDMOS). This architecture is proposed to improve the breakdown voltages and suppress the self-heating effects compared to the buried oxide double step (BODS) structure [16] made with 4H-SiC. The special on-resistances of both devices are nearly identical. The proposed SiC LDMOS device consists of double L-shaped buried oxide layers and two SiC windows. DL-SiC LDMOS show increased breakdown voltages and reduced self-heating effects using the electric field modulation technique.

2. Device structure

In this paper, the breakdown voltage and the self-heating effect of both the DL-SiC LDMOS and the BODS structure are studied. The cross sectional views of the double L-shaped buried oxide SiC LDMOS (DL-SiC LDMOS) and the BODS structure are shown in Fig. 1. The parameters for the proposed device are the following: an L-shaped buried oxide thickness of $T_{BOX} = 1$ μm, an oxide pillar height of $T_L = 1$ μm, an SiC film thickness of $T_{SiC} = 0.5$ μm, with $T'_{SiC} = T_{SiC} + T_L$, a gate oxide thickness of $T_{OX} = 0.03$ μm, a SiC window length of $L_W = 4$ μm; the length from the gate field plate to the drain field plate is $L = 10$ μm, the first L-shaped buried oxide length (L_1) and the second L-shaped buried oxide length (L_2) are $L_1 = L_2 = 3$ μm, and the gate field plate length is $L_{FP} = 2$ μm. The drift region doping concentration is $N_{drift} = 8 \times 10^{16}$ cm^{-3}, the channel doping concentration is $N_C = 4 \times 10^{17}$ cm^{-3}, and the p$^-$-substrate doping concentration is $N^-_{p\text{-}sub} = 7 \times 10^{15}$ cm^{-3}. The BODS structure has the same parameters, except for the buried oxide length, which is $L_1 = L_2$ [16].

All simulations were carried out using the 2-D device simulator, Atlas, Silvaco TCAD [23]. The threshold voltages (V_{th}) of both DL-SiC LDMOS and BODS are 5.5 V. In order to achieve realistic results, several models are used in the simulation including the “BGN” model for high doping concentration, the “SRH” model for Shockley-Read-Hall recombination, the “Auger” model for auger recombination, the “Impact Selb” model for impact ionization, the “Fldmob” model for parallel electric field dependent mobility, the “Analytic” model for concentration and temperature dependency, the “Incomplete” model for incomplete ionization, the “CVT” model for mobility including doping concentration, temperature and transverse electric field, and the “Lat.temp” model for lattice heating [24,25].

3. Simulation results and discussion

3.1. Breakdown voltage for both devices

Fig. 2 shows the region doping concentration dependency of the breakdown voltage (V_B) for the proposed DL-SiC LDMOS and the BODS structure. In this paper, the breakdown voltage of the devices is defined when the maximum electric field in SiC exceeds 3 MV/cm or the maximum electric field in silicon dioxide (SiO_2) is higher than 10 MV/cm [26]. From Fig. 2, the values of the drift region doping concentrations for both the proposed DL-SiC LDMOS and the BODS structure increase from 7×10^{16} cm^{-3} to 8.5×10^{16} cm^{-3}. The proposed DL-SiC LDMOS has more advantages for V_B than the BODS. The simulated devices show a peak breakdown voltage when the drift doping concentration is 8×10^{16} cm^{-3} and the reduced surface field (RESURF) is satisfied. The maximum breakdown voltages of DL-SiC LDMOS and BODS are 1220 V and 920 V respectively. Since both devices obtain the maximum breakdown voltages for the same N_{drift}., the special on-resistances of both devices are nearly identical (DL-SiC LDMOS: $R_{on\text{-}sp} = 18.79$ mΩ cm^2, BODS: $R_{on\text{-}sp} = 18.59$ mΩ cm^2). Fig. 3 shows the simulated electric field distributions of the DL-SiC LDMOS and BODS devices along the BB′ cut line located at 0.001 μm from the surface of the drift region shown in Fig. 1. In Fig. 3, there are two electric field peaks in the drift region for the proposed device. The inherent electric field peak (P_1) is close to the channel region, while the additional electric field peak (P_2) is close to the drain region.

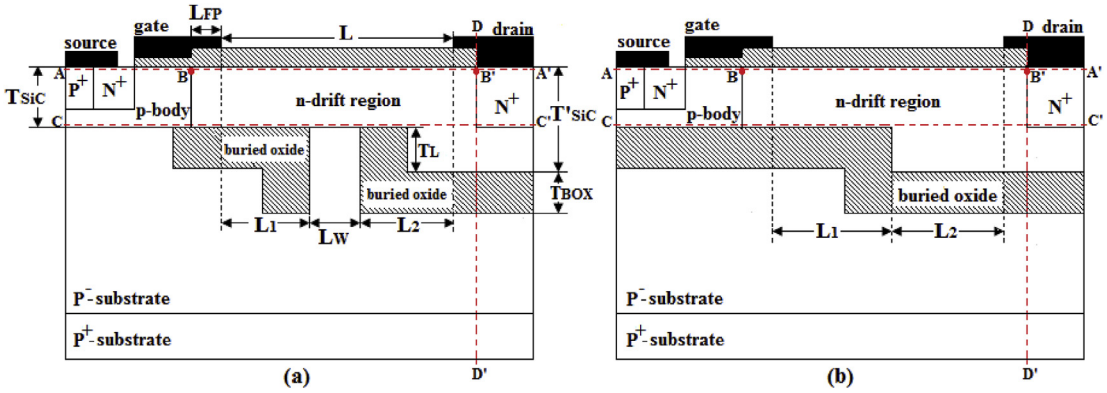

Fig. 1. Cross-section of (a) the DL-SiC LDMOS and (b) the BODS structure.