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Superior electrical characteristics of novel nanoscale MOSFET with embedded tunnel diode

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ABSTRACT

Metal Oxide Semiconductor Field Effect Transistors (MOSFET) play an important role in electronic industry development. To improve the electrical characteristics of these transistors in this paper, a new structure is proposed to reduce floating body effect, lattice temperature, and short channel effects. The main mechanism for controlling these critical issues is using an embedded tunnel diode. The tunnel diode formed by heavily doped N and P silicon windows which are embedded into the buried oxide layer. The accumulated holes are effectively released by the tunnel current of the tunnel diode. The simulation with ATLAS simulator shows that the proposed structure works properly and the important parameters such as subthreshold slope, off current, voltage gain, and maximum lattice temperature improve in comparison with the conventional nanoscale MOSFET.

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1. Introduction

During the last decades, scientists have attempted to apply small dimension devices in integrated circuits (IC) achieving high capability circuits [1–3]. Their tendency moves through nanoscale regime [4]. One of the important devices which play a key role in ICs is Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [5]. Making nano MOSFETs and applying them may force some disadvantages like short channel effects (SCE). For extending the capability of devices, the device active region can be fabricated on an insulator layer [6,7]. This technology is called Silicon On Insulator (SOI) which can improve parasitic capacitance, leakage current, and power consumption. However, applying the insulator layer has some disadvantages like floating body and self-heating effects [8–10]. In the last years, some methods have been proposed to modify the SOI MOSFET behavior [11–13]. Last methods use a window different from the active layer subjected to the insulator layer [14,15]. But, the windows were small which could not effectively improve the electrical performances such as lattice temperature, threshold voltage, off current, and subthreshold slope. In another vision, the window's materials were different from the transistor's material that make the fabrication problems.

In this paper, a novel structure of SOI MOSFET is proposed to improve its electrical characteristics. The heart of the proposed structure is a tunnel diode. The tunnel diode is embedded in the buried oxide and formed by heavily doped N and P silicon windows. A N^+ window is considered under the source region and a L-shape P^+ windows is inserted under the channel and extended under the drain region. Therefore, the proposed structure is called Double Silicon Window MOSFET (DSW-

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MOSFET). This strategy effectively improves the device performance in three different terms. One is related to reducing self heating effect. The thermal conductivity of Si is more than SiO_2. So, the created heat in the active layer of the device can pass through the silicon windows and self heating effect improves. The second term is controlling the floating body effect. Floating body effect causes main problems such as unexpected drain current, threshold voltage variation, and higher DIBL in the nano-scale device. In the proposed structure, the accumulated holes in the channel region that are created due to the impact ionization can be transferred to the substrate achieving reduced floating body effect. This behavior is due to the creation of a tunnel-diode between N^+ and P^+ windows and the narrow tunneling width between these two regions. The third one is the diminished short channel effects. Low drain induced barrier lowering (DIBL) is due to the lower floating body effect in the device. The simulation with two-dimensional ATLAS simulator shows that the proposed structure has better performance than the conventional SOI-MOSFET (C-MOSFET) in the case of leakage current, off current, maximum lattice temperature, suthreshold slope, and voltage gain [16].

The rest of the paper is as follows. In Section 2, the new structure is proposed, the discussion about the results is considered in Section 3. The consideration for achieving a perfect device is discussed in Section 4. Finally the paper is concluded in Section 5.

2. The proposed structure

The schematic cross section of the proposed structure (DSW-MOSFET) is plotted in Fig. 1. The figure shows that two silicon windows (P^+ and N^+) are considered under the channel and source regions instead of a part of the buried oxide layer. The N^+ window is considered under the source region and L-shape P^+ window is created under the channel and drain regions. The type of each window is the same as above layer. In the next section, it is shown that how this strategy improves the device

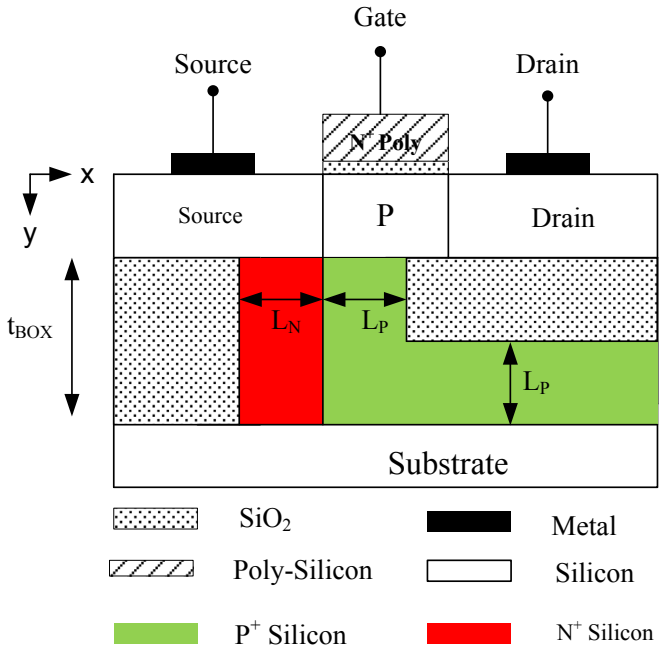

Fig. 1. The Schematic cross section of the proposed structure (DSW-MOSFET).

Table 1
The device parameters of the DSW-MOSFET and C-MOSFET used in ATLAS simulation.

Device parameters	DSW-MOSFET	C-MOSFET
Channel length	30 nm	30 nm
Length of P^+ window	20 nm	Not defined
Length of N^+ window	20 nm	Not defined
Doping density of N^+/P^+ window	1×10^{20} cm^{-3}	Not defined
Gate oxide thickness (t_{ox})	1 nm	1 nm
Buried oxide thickness	40 nm	40 nm
Source/Drain doping concentration	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Channel doping concentration	1×10^{18} cm^{-3}	1×10^{18} cm^{-3}
Top silicon layer thickness	20 nm	20 nm

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