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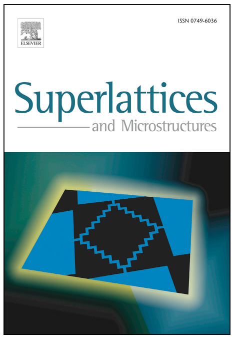

A novel gate and drain engineered charge plasma tunnel field-effect transistor for low sub-threshold swing and ambipolar nature

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A Novel Gate and Drain Engineered Charge Plasma Tunnel Field-Effect Transistor for Low Sub-Threshold Swing and Ambipolar Nature

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Abstract

In this paper, we focus on the improvement of figures of merit for charge plasma based tunnel field-effect transistor (TFET) in terms of ON-state current, threshold voltage, sub-threshold swing, ambipolar nature, and gate to drain capacitance which provides better channel controlling of the device with improved high frequency response at ultra-low supply voltages. Regarding this, we simultaneously employ work function engineering on the drain and gate electrode of the charge plasma TFET. The use of gate work function engineering modulates the barrier on the source/channel interface leads to improvement in the ON-state current, threshold voltage, and sub-threshold swing. Apart from this, for the first time use of work function engineering on the drain electrode increases the tunneling barrier for the flow of holes on the drain/channel interface, it results into suppression of ambipolar behavior. The lowering of gate to drain capacitance therefore enhanced high frequency parameters. Whereas, the presence of dual work functionality at the gate electrode and over the drain region improves the overall performance of the charge plasma based TFET.

Keywords: Ambipolar conduction, charge plasma, sub-threshold swing, gate to drain capacitance, work function engineering.

1. Introduction

Continuous increase in the chip density, leakage current, high device operation speed, and no further possibility of reduction in the sub-threshold swing (beyond the limit of 60 mV/decade) leads to increment in the power dissipation, higher packing and cooling cost [1]-[5]. The dynamic power dissipation strictly depends on the speed of operation and supply voltage, whereas static power consumption depends on the leakage current including supply voltage [6]. In current scenario, the power dissipation (dynamic + static) can be reduced only by operating the device at very low supply voltage. As a solution of ultra-low power devices, tunnel field-effect transistor is proposed and studied widely in recent years [7]-[9]. Apart from the ability of operation in ultra-low voltage range, it offers the very low leakage current, sub-threshold swing (SS) below the fundamental limit of the conventional metal oxide semiconductor field-effect transistor ($\frac{kT}{q}\approx$60 mV/decade) [10]. With all these advantages, it suffers from the low-current driving capability, conduction for the positive (PMOS) as well negative (NMOS) gate voltage and degraded high frequency response of the device. To add benefits related to fabrication of device, a doping-less tunnel field-effect transistor is proposed [11]-[17] which uses the appropriate value of work function contacts over the drain and source region to induce n+ and p+ regions instead of using conventional diffusion, ion implantation and thermal annealing techniques. This process is relatively simple as contrast to conventional doping processes and shows very less random dopant fluctuation effect [16]. This charge plasma TFET also suffers from the same issues like conventional doped TFET of ambipolar conduction, low ON-state current and poor RF performance [18]. For solving these problems, various methods are proposed as follows.

1. Use of heterojuntion material (wider bandgap material for drain region and narrow bandgap material for the

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