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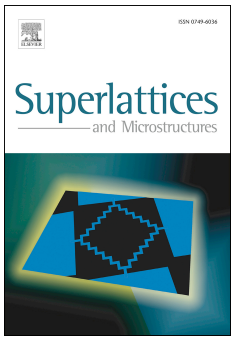

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Impact of Asymmetric Dual-*k* Spacer in the Underlap Regions of sub 20nm NMOSFET with Gate Stack

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ABSTRACT

This paper shows the systematic study of underlap double gate (U-DG) NMOSFETs with Gate Stack (GS) under the influence of dual-*k* spacers at the different underlap regions. In highly scaled devices, underlap is used at the Source and Drain side so as to reduce the short channel effects (SCE's) but at the cost of low on current (I_{ON}) and increased channel resistance. The high-*k* spacers are used to counter this problem. The I_{ON} is improved but at the cost of highly enhanced parasitic capacitances. This paper explores the possibility of using asymmetric dual-k spacer at the source underlap side so as to counter the shortcomings of high-*k* spacers in highly scaled devices on the basis of analog parameters: I_{ON}, g_m, gm/I_D, and intrinsic gain, gmR_o and RF performance in terms of parasitic gate capacitance (C_{gs}, C_{gd} and C_{gg}),gate to source/drain resistances (R_{gs} and R_{gd}), transport delay (τ_m), the unity current gain cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}).A single stage amplifier performance is also analyzed where it has been seen that the asymmetric dual-k spacer at the source underlap side gives better performance as compared to the other devices under comparison.

Keywords: Gate Stack; dual-*k* spacer; fringing fields; I_{ON}; intrinsic capacitances.

I. INTRODUCTION

With recent advancement in the field of the MOS technology, the devices are scaled down to nanometers realm [1]. The Short Channel Effects (SCEs) [2] comes into effect with such miniaturization of the devices. The Double Gate Underlap MOSFET (U-DG) emerges as one of the potential solution providing immunity against SCE's such as Drain Induced Barrier Lowering (DIBL) [3], the Gate Induced Drain Leakage (GIDL) [4] and the fringing capacitance [5]. However, it comes at the cost of increased effective channel resistance and decreased on current (I_{ON}). The underlap length have been optimized using with respect to on current to off current ratio (I_{on}/I_{off}) [6]-[11].
In an effort to increase the I_{ON}, the Oxide Capacitance (C_{ox}) is increased by reducing the oxide thickness (t_{ox}). But gate oxide of 1.2nm [12] is an absolute necessity to prevent gate quantum mechanical tunneling [1] [13] [14] with SiO_2 as the gate dielectric material. Therefore, high-*k* materials (HfO_2, Al_2O_3 etc.) [15] [16] are used as gate oxide.