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Symmetrical SOI MESFET with a dual cavity region (DCR-SOI MESFET) to promote high-voltage and radio-frequency performances

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ABSTRACT

A novel symmetrical SOI-MESFET is reported to enhance high-voltage and radio-frequency performances, successfully. Two p-type cavity regions with certain features are embedded in the proposed structure to control the channel region. The cavity regions absorb the channel potential lines resulting in an evener potential profile throughout the channel region. Hence, the critical electric field at the end of gate edge near the drain will be considerably reduced thus increasing the breakdown voltage, finally. A comprehensive comparison in terms of breakdown voltage, radio-frequency parameters, drain-source conductance and minimum noise figure shows that the reported new device reaches a superior electrical performance when compared with a conventional SOI MESFET.

1. Introduction

Devices based on the technology of silicon-on-insulator (SOI) are very well-suited candidates for high-voltage and high-frequency operations [1–4]. Lower parasitic capacitances, high latch-up immunity and powerful isolation caused by buried oxide enable the SOI-MESFET to operate as a high-voltage, high-frequency and high-speed device [5–7]. In comparison to other technology such as laterally diffused MOSFET (LDMOS), SOI-MESFET provides a more cutoff frequency and a more maximum oscillation frequency [8–10]. Therefore, SOI-MESFET structure is considered as a powerful device for important applications such as military communications, storage data and satellites [11,12].

Regarding to the SOI-MESFET structure, high capability of operating in high-power and high-frequency applications causes many efforts reported to promote the electrical performance of a SOI-MESFET device [13–17].

Using a metal plate in the buried oxide and also on the device surface has been proposed as an interesting solution to absorb the critical electric field thus resulting in decrease in the breakdown voltage [18,19].

Utilizing the filed plate is introduced to as an effective method in order to enhance the breakdown voltage of the SOI MESFETs [20]. A new high voltage device with an enhanced breakdown voltage and a reduced specific on-resistance has been reported. The structure features a drain vertical field plate and a gate vertical field plate (DTDP SOI). The distribution of electric field in the drift region is modulated and the average electric field strength is enhanced, resulting in the improvement in the breakdown voltage.

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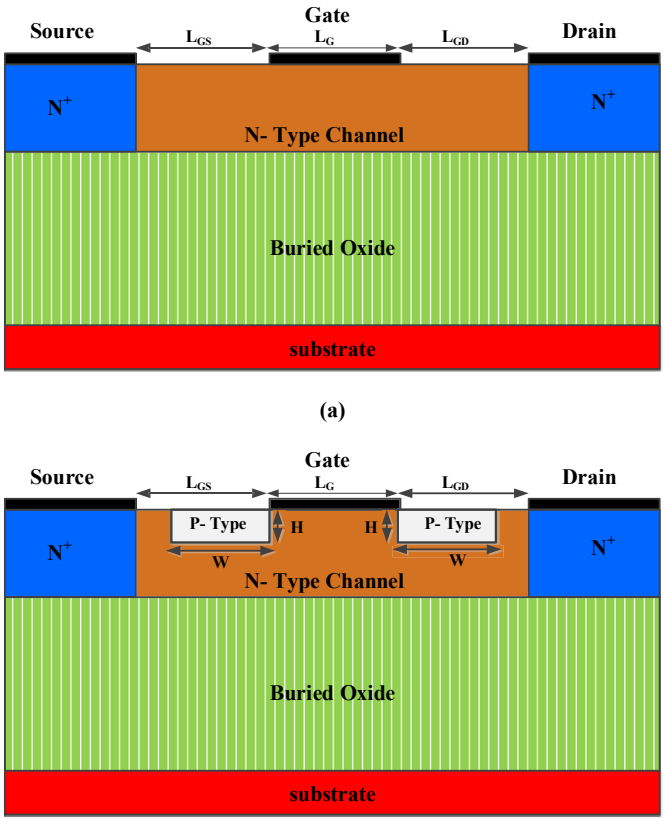

Fig. 1. A schematic cross-sectional view of the proposed structure implemented in SILVACO simulator.

An improved 4H–SiC power MESFET with double source field plates (DSFP) for high-power applications is proposed (DSFP-MESFET) [21]. The DSFP structure significantly modifies the electric field in the drift layer. The influence of the DSFP structure on saturation current, breakdown voltage, and small-signal characteristics of the DSFP-MESFET were studied by numerical device simulation.

In another research, a novel double-recessed 4H-SiC MESFET with metal plate (MP) termination technique and recessed source-drain drift region is introduced and its electrical performances are studied by two dimensional numerical simulations [22]. The MP modifies the electric field in the channel and modulates the surface electric field distribution leading to the further enhancement of the breakdown voltage.

A GaAs MESFET with multi-recessed drift region and partly p-type doped space layer (MPS-MESFET) is proposed and DC and RF characteristics are analyzed by 2D numerical simulation [23]. The multi-recesses eliminate the spaces adjacent to gate and stop the depletion region extending towards drain and source. Also by using a partly p-type doped space layer, the GaAs MESFET performance is further improved.

Recently, a new technique has been introduced to scatter the electric field inside the channel region. Two trench with different materials are embedded inside the channel and the buried oxide regions to modify the configuration of the potential profile. As a result, high breakdown voltage and high driving current are obtained owing to utilizing the trenches [24].

This work presents a new effort to solve the concerns about the conventional SOI-MESFET. The technique we have addressed in this paper is pushing the potential lines toward the source and drain regions, simultaneously. Two p-type cavity regions are created in gate-source spacing and gate-drain-spacing. The cavity regions successfully absorb the potential lines toward itself thus increasing the breakdown voltage and radio-frequency performances. The comparison of device under study with a conventional SOI MESFET shows that the proposed structure has enhanced the critical parameters in terms of breakdown voltage, drain-source conductance, parasitic capacitances, radio-frequency parameters and minimum noise figure, considerably.

The organization of this work is done in 5 sections. The first section, we are now studding it, is about the introduction of the paper. The second section describes the configuration of the proposed device. A comprehensive comparison between the device under the study and the conventional device is presented in the third section. The fourth section provides a useful