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Superlattices and Microstructures

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Growth of IZO/IGZO dual-active-layer for low-voltage-drive and high-mobility thin film transistors based on an ALD grown Al_2O_3 gate insulator



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ARTICLE INFO

Article history:

Received 27 August 2014

Received in revised form 7 October 2014

Accepted 8 October 2014

Available online 16 October 2014

Keywords:

Thin-film transistors

Dual-active-layers

Atomic layer deposition

Density-of-states

ABSTRACT

We successfully integrated the high-performance oxide thin film transistors with novel IZO/IGZO dual-active-layers. The results showed that dual-active-layer (IZO/IGZO) TFTs, compared with single active layer IGZO TFTs and IZO TFTs, exhibited the excellent performances; specifically, a high field effect mobility of $14.4 \text{ cm}^2/\text{Vs}$, a suitable threshold voltage of 0.8 V , a high on/off ratio of more than 10^7 , a steep sub-threshold swing of 0.13 V/dec , and a substantially small threshold voltage shift of 0.51 V after temperature stress from 293 K to 353 K . In order to understand the superior performance, the density-of-states (DOS) were investigated based on the temperature-dependent transfer curves. The superior electric properties were attributed to the smaller DOS and higher carrier concentration. The proposed IZO/IGZO-TFT in this paper can be used as driving devices in the next-generation flat panel displays.

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1. Introduction

Currently, amorphous gallium–indium–zinc–oxide (a-IGZO) thin-film transistors (TFTs) receive considerable attention and attract increasing research interest owing to their potential application in active-matrix flat-panel displays (AMFPD) [1–3] as they have various advantages such as good short-range uniformity, high field effect mobility, high transparency, low cost, low temperature fabrication process. However, unfortunately, the increase in the Ga composition deteriorates the mobility and the carrier concentration. As more functions of peripheral circuits are integrated into AMFPD panels, TFTs in them require higher mobility. The mobility and threshold voltage of the TFTs are well known to be strongly related to the carrier concentration of the TFTs' active layer materials [4]. Motivated by this background information, this work used an IZO/IGZO dual-active-layer to obtain a high mobility as IZO could provide high carrier concentration.

For switching TFTs in AMFPD panels, the stress-induced threshold voltage shift (ΔV_{TH}) is a very challenging issue that must be taken into account in a pixel circuit design. The origin of the instability of oxide-TFTs has commonly been attributed to the threshold voltage (V_{TH}) being shifted by charge trapping/de-trapping at the gate interface (gate insulator/channel layer) [5], accumulation of photo generated carriers or defects at the gate interface [6], and thermally activated charge carriers [7]. In order to obtain a good channel/insulator interface, good-quality Al_2O_3 thin films with a small root-mean-squared (RMS) roughness (0.46 nm) were deposited via ALD technique and used as gate insulators. ALD enables the growth of highly conformal, large-area films with high-precision thickness control [8], which makes it an attractive technique for the large-scale fabrication of both the semiconductor and dielectric materials in TFTs. The oxide TFTs which use ALD-fabricated Al_2O_3 as gate insulator exhibit remarkably high and stable performance [9].

In the present work, high-performance TFT with IZO (5 nm)/IGZO (17 nm) dual-active-layer (device B) was fabricated, showing a mobility as high as that of the TFT with IZO (22 nm) single layer (device C) and a stability as high as that of the TFT with IGZO (22 nm) single layer (device A). In order to understand the superior performance of device B, the density-of-states (DOS) were investigated based on the temperature-dependent transfer curves. Using this method to characterize DOS in dual-active-layer TFT has been reported for the first time.

2. Experiments

The device structure used in this study was a conventional bottom-gate TFT as shown in the inset of Fig. 1. The dual-active-layer was composed of two layers. One layer was the IZO with high carrier concentration and close to the gate insulator. The other layer was the IGZO which was close to of Source/Drain metal. An Al_2O_3 gate insulator approximately 150-nm-thick ($C_i = 44 \text{ nF/cm}^2$) was deposited by using alternating exposures of $Al(CH_3)_3$ and H_2O vapor at a deposition rate of 1 Å per cycle by ALD. $Al(CH_3)_3$ and H_2O were used as the sources of Al and O, respectively. The ALD Al_2O_3 gate insulator deposition temperature was fixed at 250 °C. IZO films were deposited by rf-magnetron sputtering at room temperature using an IZO target (99.99%, In_2O_3 , $ZnO = 1:1 \text{ mol}\%$) with a power density of 1 W/cm² and gas mixing ratio of Ar: O_2 (30:1). Chamber pressure before sputtering was 5×10^{-4} Pa, and total pressure was 0.5 Pa. Prior to channel layer deposition, the target was pre-sputtered in pure Ar gas for 10 min to remove the natural surface oxide layer of the target. IGZO films (99.99%, In_2O_3 , Ga_2O_3 , $ZnO = 1:1:1 \text{ mol}\%$) were deposited in the same condition. After deposition of active layer, about 200 nm Al was deposited by thermal evaporation to form the source and drain electrodes through a shadow-mask with the channel width (W) of 1000 μm and channel length (L) of 50 μm. Thermal annealing was carried out at 300 °C for 35 min in atmosphere. The thickness of the film was measured by the alpha step (Dektak 3st). The electrical characteristics of TFTs were measured with Agilent E3647A Dual output DC power supply and Keithley 6485 Picoammeter and related software. The capacitance characteristics were measured with Agilent E4980A LRC meter. Atom force microscope (AFM, nanonaviSPA-400 SPM) was used to investigate the surface properties of films.

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