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Investigation of InP/InGaAs metamorphic co-integrated complementary doping-channel field-effect transistors for logic application

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DC performance of InP/InGaAs metamorphic co-integrated complementary doping-channel field-effect transistors (DCFETs) grown on a low-cost GaAs substrate is first demonstrated. In the complementary DCFETs, the n-channel device was fabricated on the $In_xGa_{1-x}P$ metamorphic linearly graded buffer layer and the p-channel field-effect transistor was stacked on the top of the n-channel device. Particularly, the saturation voltage of the n-channel device is substantially reduced to decrease the V_{OL} and V_{IH} values attributed that two-dimensional electron gas is formed and could be modulated in the n-InGaAs channel. Experimentally, a maximum extrinsic transconductance of 215 (17) mS/mm and a maximum saturation current density of 43 (−27) mA/mm are obtained in the n-channel (p-channel) device. Furthermore, the noise margins NM_H and NM_L are up to 0.842 and 0.330 V at a supply voltage of 1.5 V in the complementary logic inverter application.

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1. Introduction

IIIV heterostructure field-effect transistors (HFETs) have been widely applied in signal amplifier and digital integrated circuits [1,2]. Among of the HFETs, the transconductance values of high electron mobility transistors (HEMTs) might be relatively high due to the two-dimensional electron gas (2DEG) modulated in channel. Nevertheless, they suffered from poor device linearity and low output current [3]. In order to improve the device linearity and reduce the higher order harmonic terms in linear amplifiers, an alterable HFET, i.e., doping-channel FET (DCFET), was investigated to exhibit broader

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gate voltage swing [4–6]. For the DCFET, a large energy-gap undoped (or low-doped) material layer as a gate Schottky barrier layer was employed to enhance the gate turn-on voltage and drain current [5]. On the other hand, as considering the carrier transport, the GaAs channel layer replaced with an InGaAs strain layer in GaAs-based HFETs is appropriate attributed that the InGaAs strain layer has lower effective electron mass, higher electron mobility, and higher peak electron velocity [6]. But, it will give rise to compressive strain, and In mole fraction as well as the thickness of InGaAs strain layer is critically limited because the lattice constant of InGaAs does n't mismatch with GaAs material. Also, the theoretical predictions and experimental results depicted that coherent layer strain could accommodate the lattice mismatch as the thickness of InGaAs layer was thinner than the critical value [7,8].

Over the past years, InP-based HFETs have attracted much attention due to the high electron mobility and saturation velocity of the InGaAs channel layer with high In mole fraction [9,10]. However, InP substrates are expensive, fragile, and easily broken during processing than the GaAs-based transistors. Recently, several InP-based metamorphic transistors grown on low-cost GaAs substrates have been investigated [11–13]. The report demonstrated that the $In_xGa_{1-x}P$ to InP metamorphic buffer layer in metamorphic heterojunction bipolar transistors can offer better thermal properties resulting in a relatively smaller thermal resistance when compared with the widely used InAlAs metamorphic buffer [11].

Furthermore, vertical monolithic integration of the HFETs by the continuous growth of successive layers permits the different devices to be optimized on the same wafer, which provides the reduction of fabrication complexity [14,15]. Among of the integrated devices, the co-integration of n- and p-channel HFETs attracted considerable attention for extremely low power dissipation in complementary logic circuits [14]. In this paper, new InP/InGaAs metamorphic complementary DCFETs on the GaAs substrate is first reported to exhibit excellent dc performance. The p-channel field-effect transistor was stacked on the top of the n-channel device grown on the $In_xGa_{1-x}P$ metamorphic buffer layer. Also, large noise margins of the complementary logic inverter are achieved.

2. Experiments

The studied InP/InGaAs metamorphic co-integrated complementary DCFETs were grown on an (100) oriented semi-insulating GaAs substrate by molecular beam epitaxy (MBE) system. The epitaxial structures consisted of a 1.5 μm undoped and linearly graded $In_xGa_{1-x}P$ (x: 0.52–1) metamorphic buffer layer, a 0.15 μm undoped InP layer, a 100 Å $n^+ = 2.5 \times 10^{17}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ n-channel layer, a 100 Å undoped InP n-channel gate layer, a 300 Å i-$In_{0.53}Ga_{0.47}As$ layer, a 200 Å undoped InP layer, a 100 Å $p^+ = 6.5 \times 10^{17}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ p-channel layer, a 80 Å undoped InP p-channel gate layer, and a 300 Å $p^+ = 1 \times 10^{19}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ cap layer. After covering the p-channel regime, the top four layers of the structure were removed by chemical wet selectively etching techniques for the fabrication of the n-channel device. Then, a mesa structure provided the required isolation to distinguish the n- and p-channel regimes. Drain and source ohmic contacts were formed by alloying the evaporated AuGeNi metal at 400 °C for 30 s. Sequentially, the n^+-InGaAs cap layer of the n-channel device and the 300 Å i undoped InGaAs layer of the p-channel device were recessed, and then the gate metal Au was simultaneously deposited on the undoped InP gate layers of both the integrated devices. The schematic cross section of the integrated devices is shown in Fig. 1. As comparing to the metamorphic n-channel device, only four layers are added in the integrated complementary DCFETs. In the two devices, the gate dimensions and the drain-to-source (D–S) spacing were 1×100 μm^2 and 3 μm, respectively.

3. Experimental results and discussion

The device performance of the n- and p- channel devices will be description below. In the InP/$In_{0.53}Ga_{0.47}As$ n-channel metamorphic DCFET, the matched material layers were deposited on the $In_xGa_{1-x}P$ linearly graded metamorphic buffer layer. After removing the top four layers of the epitaxial structure, the corresponding energy-band diagram from gate to the 0.15 μm undoped InP layer in the n-channel device at equilibrium is depicted in Fig. 2. For the presence of the considerable conduction band

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