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Investigation and study of the electrical characteristics of anodic oxide films SiO_2 annealed at various temperatures

Bécharia Nadji

Laboratoire d'Eectrification des Entreprises Industrielles, Faculté des Hydrocarbures et de la chimie, Université M'hamed Bougara Boumerdès, 35000 Boumerdès, Algeria

Abstract

The anodic silica films were produced by anodization of monocrystalline silicon wafers in pure water in an electrolysis cell (P.T.F.E), with a constant current density of 20 μA/cm^2. All anodizations are performed at room temperature. During oxidation film thickness increases linearly as a function of total charge. Films were annealed under nitrogen atmosphere at various temperatures (600, 800 and 1050 °C). MOS capacitors with anodic oxides were elaborated. This study deals to the determination of interface states density Si/SiO_2 and the study of electronic conduction. Using static, quasi-static, $C(V)$, $G(\omega)$ measurements, we have determined the interface states density, fixed charges density for annealed oxides at various temperatures. The conduction mechanism was determined with $I(V)$ measurements.

Keywords: Annealing oxidation; Pure water; Interface states density, Electrical characterisation; MOS capacitors; Fowler–Nordheim conduction

1. Introduction

The increasing miniaturization and the higher integration density in CMOS technology and the capacitive structures for memories require the fabrication of ultra thin gate oxides (lower than 10 nm). These oxides must be perfectly homogeneous, be deprived of defects such as pin-holes, with high field breakdown and present very good Si/SiO_2 interface in particular, both the interface states density and the fixed charges density must be low. In addition, the reproducibility and the homogeneity of these properties are essential factors for the reliability and the reproducibility of device performances. Moreover, the thickness of the oxide films must be precisely controlled during the fabrication process. The conventional method of high temperature oxidation hardly meets these requirements. With the progressive shrinking of LSI device size, device and circuit is complexity increasing. The fabrication process is also becoming increasingly difficult. Moreover, there is a great demand to reduce energy consumption on the grounds of preventing global warming and to environmental pollution. An oxidation process in VLSI fabrication requires a high temperature and thermal stress damages the silicon wafer inconspicuously. From this viewpoint, low temperature processes have been researched. Many low temperature processes have been proposed to fabricate insulation films on silicon such as plasma deposition [13], chemical vapour deposition (CVD), photo-CVD, jet vapour deposition JVD, anodic oxidation. However, the pollution which systematically accompanied these oxides formation had made, so far, their use unthinkable in technology. To obtain oxides free from any contamination, the anodic oxidation of silicon in pure ultra water [3,4] can be used. This is an oxidation process, which is carried out at room temperature. On the other hand, the electrochemical oxidation of silicon in pure water permits to obtain very thin homogeneous oxide layers whose thickness can be easily controlled by simple coulometry. Introducing this oxidation step into semiconductor technology would help to reduce the total thermal budget during processing. This is very important regarding dopant diffusion for example. The anodic oxide can be applied for low-temperature VLSI processes, bonded and etched SOI and oxide film for micro-machining [14]. Here, The work presented here consists of investigating and studying the electronic properties of anodic oxide film (SiO_2). This study deals to the determination of interface states density Si/SiO_2 and the study of electronic conduction. We report on the experimental method and the characteristics of anodic oxidized silicon dioxide films grown in pure water at room temperature as a possible oxidation process at a low temperature. The films were grown in pure water. For the characterization of the grown films, we systematically used the electrical methods (static, quasi-static, $C(V)$ as well as $I(V)$ measurements) [12]. Electrical characteristics of the anodic oxide film are improved by thermal annealing.

E-mail address: b_nadji@yahoo.com.

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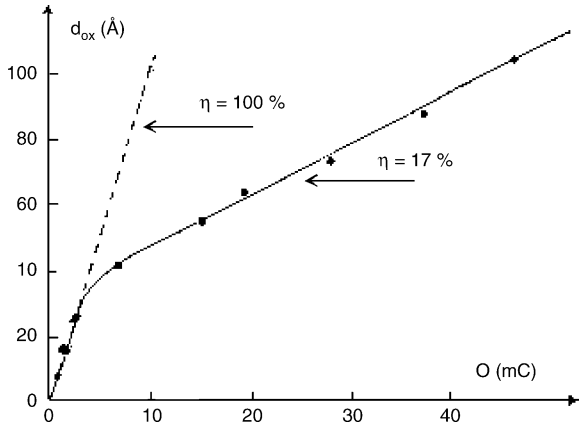

Fig. 1. Calibration curve: oxide thickness formed according to the electricity quantity in the electrochemical cell; current density = 10 μA/cm^2, surface = 1 cm^2.

2. Experimental procedure

MOS structure were fabricated on a p-type ⟨1 0 0⟩ oriented silicon substrate, doped with boron in the range 10^{15}–10^{16} cm^{-3}. After a conventional chemical cleaning, a thermal oxidation under dry oxygen is carried out in order to obtain layers from 2000 to 3000 Å. Windows are opened by lithography and the anodic oxides are grown in an electrolysis cell (P.T.F.E) with pure water under constant current density of 20 μA/cm^2. All anodizations are performed at room temperature. A given oxide thickness is obtained by stopping anodization as soon as an charge quantity defined by the calibration curve of Fig. 1 [3] has flown in the circuit. After post anodization annealing under nitrogen atmosphere at various temperatures (600, 800 and 1050 °C), an aluminium film is deposited by evaporation and annealed at 450 °C during 30 mn. The obtained $C(V)$, $G(\omega)$ characteristics were used to determine interface states densities, oxide fixed charges. The $I(V)$ characteristics are obtained either by applying voltage ramp to the sample, or by applying fixed voltage which is incremented step-by-step, and used to determine the conduction type.

3. Experimental results and discussion

3.1. Fixed charges

The presence of electric charges in the oxide results in a simple $C(V)$ ideal curve shifted along the voltage axis. The fixed charges quantity Q_f contained in the oxide is measured by comparing the experimental value of flat band voltage with the computed value starting from the relation [7,9]:

$$V_{FB}^{C} = \left[\phi_m - \chi_{sc} - \frac{E_g}{2q} - KT\,\mathrm{Ln}\left(\frac{N_A}{n_i}\right)\right] \quad (1)$$

where $q(\phi_m - \phi_{sc})$ is the barrier height between the metal and the semiconductor.

The experimental value of the flat band (V_{FB}^{e}) voltage is deduced from the gate voltage value for which the measured capacitance is equal to the structure theoretical capacitance at flat band voltage.

The density N of fixed charges is obtained using the following expression:

$$N = \frac{Q_f}{q} = \frac{\Delta V_{FB} C_{ox}}{q} \quad (2)$$

where $\Delta V_{FB} = V_{FB}^{C} - V_{FB}^{e}$.

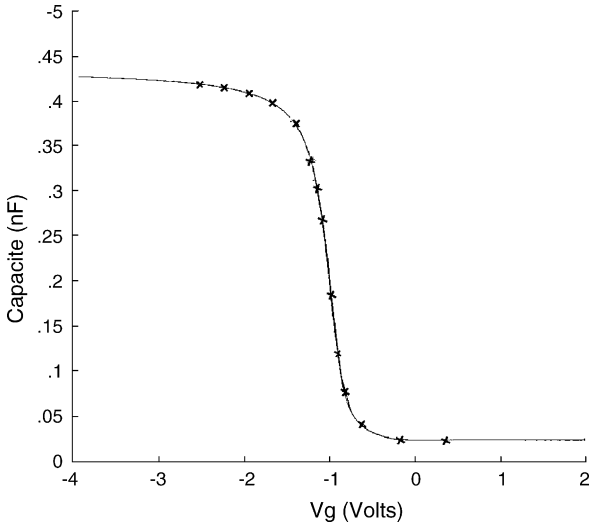

Fig. 2. Experimental capacitance (x) and theoretical curve; temperature annealing of 980 °C, surface 400 μm × 400 μm, and oxide thickness: 9 nm.

The experimental $C(V)$ characteristic of Fig. 2 is practically overlapping on the ideal characteristic.

By taking $q(\phi_m - \phi_{sc}) = 0.11$ eV, the theoretical value of flat band voltage is calculated from relation (1).

We can reasonably state that the oxide charge density in these anodic films is lower than 10^{11} cm^{-2}, which confirms that there is no appreciable pollution occurring during the anodic oxidation of silicon in pure water. It is noticed besides that the lack of sensitivity on the determination of charges is related to the low oxide thickness.

3.2. Interface states

3.2.1. Quasi-static method

The $C_{LF}(V_g)$ curve is obtained by subjecting MOS structure to a voltage ramp of small slope. This characteristic is deduced from the displacement current flowing in the circuit. Voltages were ramped from 20 to 50 mV/s. The determination of interface states density can be obtained by comparing such a curve either with a high frequency experimental curve ($C_{LF} - C_{HF}$ method) or with a theoretical curve calculated by supposing that the states do not give any contribution to the MOS structure capacitance [1].

The density of Si/SiO$_2$ interface states is given by:

$$D_{it} = \frac{C_{ox}}{q_s}\left[\frac{C_{LF}/C_{ox}}{1-(C_{LF}/C_{ox})} - \frac{C_{TH}/C_{ox}}{1-(C_{TH}/C_{ox})}\right] \quad (3)$$

3.2.2. Conductance method

This method requires the conductance measurement of the G_m and the capacitance C_m associated with the structure as a function of ω for various gate bias values V_g. According to the Nicollian model [7], this method allows the determination, at the same time, interface states density D_{it} in terms of energy and the principal parameters associated with these states (the standard deviation of the surface potential Ψ_s and the effective capture