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A novel 4H–SiC MESFET with recessed gate and channel

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ABSTRACT

New structures named as recessed gate and channel (RGC) silicon carbide (SiC) based metal semiconductor field effect transistors (MESFETs) are reported in this paper, in which the gate is recessed into the channel, and the channel is recessed into the p-buffer layer at the source and/or the drain side. Important parameters such as short channel effect, maximum DC trans-conductance (g_m), drain current, breakdown voltage and output resistance of the proposed structures are simulated and compared with the conventional 4H–SiC MESFET. Simulation results disclose that, compared to the conventional structure, the structure with recessed full gate and channel (FGC):

1. Improves the DC trans-conductance (g_m).
2. Increases the output resistance.
3. Enhances the breakdown voltage.
4. Reduces the short channel effect.

Moreover, source side recessed gate and drain side recessed channel (SG–DC) structure has higher g_m and output resistance in comparison with the conventional structure. Drain side recessed gate and source side recessed channel (DG–SC) structure has larger breakdown voltage and drain current than those of the conventional structure.

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1. Introduction

Silicon carbide metal semiconductor field-effect transistors (SiC MESFETs) are well suited for high power radio frequency (RF) applications, especially in extremely challenging environments, owing to their superior material properties. With the recent progress in SiC epitaxial material and the device process, excellent power and RF performances of SiC MESFETs have been reported [1]. The absence of gate oxide makes the MESFET device naturally immune to oxide-related problems such as radiation plasma damages and hot-carrier effects. Besides, the channel of a MOSFET device is formed by the inversion layer at the gate oxide–silicon interface, thus carriers suffer from high normal fields and serious roughness scattering, leading to drastic reduction of effective mobility and trans-conductance. However, the channel of MESFET device is formed in the undepleted bulk region which is usually near the bottom of the active layer, thus carrier mobility is less degraded. This is one of the advantages for the MESFET devices against the MOSFETs. On the other hand, since the gate of MESFET is a metal–semiconductor Schottky contact, the voltage swing is limited within a relatively small range, depending on the barrier height. Hence, the MESFET is a good candidate for low-power applications [2]. SiC MESFETs are very well-suited for high voltage, high power and high temperature applications due to its superior material properties especially high critical electrical field, high electron saturation velocity, and high thermal conductivity. The main drawback in using SiC for microwave devices lies in its poor low field electron mobility of 300–500 $cm^2/V\,s$, at doping levels of interest for MESFETs in the range of 1×10^{17}–$5 \times 10^{17}\ cm^{-3}$. This drawback results in a larger source resistance and lower trans-conductance compared to GaAs based MESFETs [3–9].

In order to improve the device performance of SiC MESFETs, various structures are proposed in the literature. Floating metal strips [7], recessed p-buffer layer [9], double recessed gate [10], multiple recessed gate [11], and un doped space barrier [12] are techniques to improve the device performance. In this article, with the purpose of improving the short channel effects, saturated drain current, breakdown voltage, DC trans-conductance and output resistance, new 4H–SiC MESFETs with recessed gate and channel (RGC) are proposed. In the following section, the proposed structures and the physical models used in the 2-D simulation are described in details. Also, in this section, fabrication feasibility of the proposed structures is investigated. In the third section, we first explain how the presence of the recessed gate and channel will reduce the short channel effects such as DIBL. Also, in this section the effect of recessed gate and channel on the drain current, electric field and breakdown voltage is studied in details. After that, the maximum DC trans-conductance and output resistance of the proposed structures are simulated and compared to that of conventional structure.

2. Device structure and fabrication feasibility

2.1. Device structure

Fig. 1a–d shows the schematic cross-section of the source side recessed gate–drain side recessed channel (SG–DC), drain side recessed gate–source side recessed channel (DG–SC), recessed full gate and channel (FGC) and conventional [9] structures respectively. The dimensions of the four structures are as follows: gate length $L_g = 0.7\ \mu m$, gate–drain spacing $L_{gd} = 1\ \mu m$, gate–source spacing $L_{gs} = 0.5\ \mu m$, channel thickness $T_C = 0.25\ \mu m$, and the channel doping $N_D = 3 \times 10^{17}\ cm^{-3}$. The doping and thickness of the p-buffer layer are $N_A = 1.4 \times 10^{15}\ cm^{-3}$ and $T_P = 0.5\ \mu m$, respectively. A compensation-doped (vanadium) semiconductor is used for semi-insulating substrate. Nickel is chosen for the gate Schottky contact with a work function of 5.1 eV and aluminum is used for the source/drain contacts. For all of the structures, recessed gate depth into channel and recessed channel depth into p-buffer layer are 0.05 μm. Recessed gate and channel length for SG–DC and DG–SC structures are 0.35 μm, but, recessed gate and channel length for FGC structure is 0.7 μm. The devices are simulated using two dimensional device simulator ATLAS software [13] with SiC material parameters [14–16]. In order to achieve more realistic results, several models are activated in simulation, including the 'SRH' model for Shockley–Read–Hall recombination, the 'Conmob' model for standard concentration dependent mobility, the 'Fldmob' model for parallel electric field-dependent mobility, the 'Fermi Dirac' model for statistics and the 'Impact Selb' model for impact ionization [17].