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An analytical threshold voltage model for a short-channel dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET

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ABSTRACT

In this paper, an analytical short-channel threshold voltage model is presented for a dual-metal-gate (DMG) fully depleted recessed source/drain (Re-S/D) SOI MOSFET. For the first time, the advantages of recessed source/drain (Re-S/D) and of dual-metal-gate structure are incorporated simultaneously in a fully depleted SOI MOSFET. The analytical surface potential model at Si-channel/SiO_2 interface and Si-channel/buried-oxide (BOX) interface have been developed by solving the 2-D Poisson's equation in the channel region with appropriate boundary conditions assuming parabolic potential profile in the transverse direction of the channel. Thereupon, a threshold voltage model is derived from the minimum surface potential in the channel. The developed model is analyzed extensively for a variety of device parameters like the oxide and silicon channel thicknesses, thickness of source/drain extension in the BOX, control and screen gate length ratio. The validity of the present 2D analytical model is verified with ATLAS™, a 2D device simulator from SILVACO Inc.

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1. Introduction

In the era of sub-100 nm device dimensions, continuing conventional MOSFET scaling and keeping up with the ITRS roadmap are proved to be more difficult than ever. This is attributed to the acute short-channel-effects (SCEs) in the shrinking nanometer order [1,2]. In the conventional MOSFET, as

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the channel length diminishes, the gate control over the channel gets reduced due to the increased source/drain capacitances [3]. The SCEs thereby lead to the least reliable device characteristics, such as threshold voltage, with decreasing channel length. Many other problems in the conventional MOSFET associated with SCEs are degradation of subthreshold slope, decreasing I_{on}/I_{off} ratio, a lack of pinch-off, drain-induced-barrier-lowering (DIBL) and hot-carrier effect at increasing drain voltage [4–9].

However, a potential candidate to continue the MOSFET scaling further is the fully-depleted silicon-on-insulator (FDSOI) MOSFET. Rigorous research of the FD SOI MOSFETs revels that this transistor possesses higher transconductance [6–8], lower threshold voltage roll-off and steeper subthreshold slope [6–9] compared to the bulk MOSFET. In the FD SOI MOSFETs, the front channel parasitic junction (source/drain to channel) capacitances reduces resulting in higher switching speeds [10]. The presence of the buried oxide (BOX) further suppresses drawbacks like leakage current [6,7], threshold voltage roll-off [9–11], higher sub-threshold slope [11] and body effect [6–11]. However, due to the ultra thin source and drain regions, FD SOI MOSFETs possess large series resistance which leads to the poor current drive capability of the device despite having excellent short-channel characteristics. The recessed source/drain (Re-S/D) ultrathin body (UTB) SOI MOSFET was proposed and fabricated by Zhang et al. [12] to overcome this large series resistance problem. In the Re-S/D UTB SOI MOSFETs, source and drain regions are extended deeper into the buried oxide (BOX) to minimize their resistance contribution in total series resistance of the device. Svilicic et al. [13] presented an extensive analysis of this phenomenon by developing a short-channel threshold voltage model for Re-S/D UTB SOI MOSFETs. An important observation made by the analysis is that the back-channel sets in an early inversion before the onset of the front-gate inversion in *n*+-polysilicon-gated MOSFETs.

The current drive capability of Re-S/D UTB SOI MOSFETs can be made better by adopting the dual-metal-gate (DMG) structure [14] in place of the conventional single-metal-gate-structure. Long et al. [14] have proposed the dual-metal-gate (DMG) structure wherein the two gate materials are cascaded such that the source side gate metal (M_1) has a relatively higher work function than the drain side metal (M_2). The structure provides the benefits of high electron velocity and enhanced source side electric field resulting in increased carrier transport efficiency in the channel region [15]. The DMG structure has been successfully employed in the conventional and SOI MOSFETs for controlling the HCE through optimizing the control gate to screen gate length ratio [4,16] without losing gate control over the channel. The DMG structure creates a step-like channel potential profile which ensures screening of the minimum potential point from drain voltage fluctuations. Thus, the metal gate M_2 behaves as the *Screen Gate* (L_2) and the metal M_1 as the *Control Gate* (L_1).

In this work, the concept of dual-metal-gate (DMG) is adopted in order to include its implicit advantages in the Re-S/D UTB SOI MOSFETs structure. To sum it all, the proposed dual-metal-gate (DMG) Re-S/D UTB SOI MOSFETs device has higher on-current density, lower DIBL and better HCE. However, the subthreshold behavior of the proposed device also needs to be inquired to assess the overall performance of the device as the knowledge of strong and weak inversion behaviors is equally important. Threshold voltage is a vital subthreshold characteristic of a MOSFET device and hence the same is modeled for the proposed dual-metal-gate (DMG) Re-S/D UTB SOI MOSFETs in the present work. For this purpose, the surface potentials are obtained at Si-channel/SiO_2 interface (the front-channel surface potential) and Si-channel/buried-oxide (BOX) interface (back-channel surface potential) by solving the 2D Poisson's equation in the channel region of the proposed device with the appropriate boundary conditions along with the assumption of parabolic potential approximation in the vertical direction of the channel. The thus obtained surface potentials are utilized to model the threshold voltage of the device. A thorough analysis is undertaken on the surface potential and threshold voltage by varying device parameters like the oxide and silicon thickness, thickness of source/drain extension in the BOX, control and screen gate length ratio. The DIBL analysis is also made in the present work. The developed model is well supported by the simulation from the 2-D numerical simulator ATLAS™ from Silvaco Inc [17] which shows a high accuracy of the developed models.

2. Device structure

Fig. 1 shows the cross-sectional view of the dual-metal-gate (DMG) Re-S/D UTB SOI MOSFETs. The entire Si channel is considered to be fully depleted to avoid floating body effect. The position along the

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