Core–shell heterojunction solar cells on silicon nanowire arrays

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ABSTRACT

Efficient core–shell TCO/a-Si/Si nanowires (SiNWs) heterojunction solar cells were fabricated on SiNW arrays prepared by metal assisted wet chemical etching of an n-type silicon wafer. The silver catalyst was carefully removed after the etching by a three-step procedure. A stack of intrinsic and p-type amorphous-Si (a-Si) was deposited as a shell onto the SiNW arrays by plasma enhanced chemical vapor deposition (PECVD), and finally, a ∼200 nm TCO layer was deposited on top of the a-Si layer by atomic layer deposition (ALD). No shunt was detected in our cells, which was a big problem in the cells prepared on similar substrates published in the literature. The core–shell heterojunction solar cells on nanowire arrays also show great improvement of the performance in comparison with those published previously. In a mesa-structured solar cell with contact area of 7 mm^2, an open circuit voltage of 476 mV, short circuit current density of 27 mA/cm^2, filling factor of 56.2% and conversion efficiency of 7.29% was determined at AM 1.5. Electron beam induced current (EBIC) measurements were performed on the solar cells, which demonstrate unambiguously that the nanowire arrays work as active photovoltaic components.

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1. Introduction

Silicon nanowires (SiNWs) as active components for photovoltaic applications have received great attention in the last few years. On one hand light absorption is greatly enhanced by light trapping [1,2], enabling reasonable absorption within a thin nanowire layer, thus reducing significantly the amount of materials used and highly efficient nanowire based solar cells comparable with wafer cells could be realized in the future. On the other hand, the requirement on the material quality for such cells is less critical [3,4], so lower grade silicon materials may be tolerable for solar cell fabrication, which would reduce the cost of the solar cells significantly.

To make a solar cell from nanowire arrays, a p–n junction has to be realized. This can be done in an axial [5,6] or in a radial [7–9] configuration. In the axial configuration, the p–n junction is realized along the length of the nanowires, either by changing to opposite dopant gas during the growth of the nanowires by CVD process or by etching with the p–n junction already present in the original wafers. A big challenge for axial configuration is the passivation of the huge surface to suppress surface recombination. In the radial configuration, SiNWs are covered by a shell of oppositely doped silicon. The radial p–n junction [1] or so-called core–shell [7] configuration has many advantages in comparison

with the axial one, because the generated electron hole pairs in the SiNWs just need to diffuse a very short length (less than the diameter of the nanowires) in the radial direction to reach the space charge region, and will be separated by the electrical field of the p–n junction immediately, thus the recombination loss of carriers during the diffusion is drastically reduced. That's why most of the effort was paid on the core–shell configuration.

In a pioneering work, Tian et al. [7] reached a conversion efficiency of 3.4% by a core–shell solar cell made on a single SiNW with a p–i–n structure, which was prepared by changing the doping gas precursors during the CVD growth process to ensure a growth in radial direction for the oppositely doped shell. An alternative way to make the p–n junction is by diffusion of doping atoms in a furnace. This, however, usually results in an undefined junction depth, in some cases even completely highly doped nanowires are formed, and the nanowires cannot work as active photovoltaic component. In a nanowire based solar cell with p–n junction prepared by a 5 s rapid thermal process at 900 °C for the dopant drive-in, conversion efficiency of only 1.47% has been reported recently for diffused p–n junction solar cells [4].

Despite of an enhanced light absorption by the SiNW arrays, the reported solar cell conversion efficiencies are rather small [4,10], suffering mainly from low open circuit voltages and shunting. Such behavior may closely be related to metal contamination from the catalyst used in preparing the nanowire arrays. To better understand this point, one should have a close look on the preparation of the SiNW arrays. There are two main methods

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for preparing SiNW arrays, either by chemical vapor deposition (CVD) using metal droplets as catalyst in the vapor liquid solid (VLS) mechanisms [11,12], or by metal assisted wet chemical etching into silicon wafers [13]. Both methods use metals as catalyst for the preparation of the SiNW arrays. In the VLS growth, the metal catalyzes the dissociation of silane, so silicon atoms dissolve in the melt, the nanowires begin to grow when silicon is saturated in the melt, while in the metal assisted wet chemical etching process, the metal catalyzes the oxidation of silicon.

Even if the catalyst is removed after the preparation of the nanowire arrays, one should be aware that traces of metal impurities may be present in the nanowires or at the surface of the nanowires due to insufficient cleaning. Metal impurities form deep level energy states in the band gap of silicon [14], and degrade significantly the lifetime of the carriers. Metal impurities at the surface of the nanowires, where later on the p–n junction is located, increase dramatically the recombination at the junction, when they are in form of metal particles, even leading to shunting of the solar cells.

It is noted that metal impurities as one of the main reasons for the low performance of the nanowire based solar cells is supported in the literature. Using sophisticated deep reactive ion etching technology [10], which is free from metal contamination, nanowire based solar cells with efficiency of 5.3% has been reached. For thick wires with diameter of 7.5 μm prepared by similar process, open circuit voltages of 600 mV and conversion efficiency up to 8.7% have been reported recently [3].
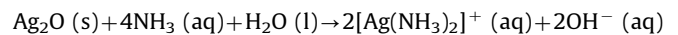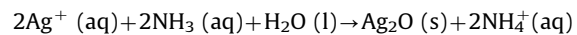
The most cost-effective way to produce SiNW arrays is metal assisted electroless wet chemical etching [13] of silicon wafers or multicrystalline silicon thin films [6], for which a HF (5 M):AgNO$_3$ (0.02 M)=1:1 (by volume) solution was used. During the etching, silver particles form and deposit on the surface of the silicon substrate. The silver particles catalyze oxidation of the silicon locally, and the HF solution removes the resulting silicon oxide successively. In this way, holes in the size of the silver particles form, usually in the range of several tens of nm. Free-standing nanowires can be formed by prolonged etching. Along with the etching of the Si wafer, Ag particles grow out of the holes and form dendrites on the sample surface. After nanowire etching the Ag nanoparticles stay in the holes and have to be removed, usually by an additional etching in concentrated HNO$_3$. However, due to surface tension, HNO$_3$ cannot easily penetrate into the holes between the nanowires.

In this work, we have intensively investigated the cleaning procedure for removal of silver contamination after metal assisted wet chemical etching of nanowires. A three-step cleaning procedure has been developed to remove the silver contamination, considering the high surface tension between the neighboring nanowires, surfactant was added to reduce the surface tension, in order to remove the Ag particles at the bottom of the SiNW arrays. By applying the cleaning procedure, efficient TCO/a-Si/Si nanowires (SiNWs) heterojunction solar cells have been successfully realized by depositing oppositely doped hydrogenated amorphous silicon (a-Si) shell on the crystalline core. Such heterojunction structure have many advantages due to low temperature processing [15,16] by the plasma enhanced chemical vapor deposition (PECVD), a better determination of junction and a better interface passivation by hydrogen, and are known to give higher open circuit voltages [15,17] as compared to a p–n homo-junction. A great improvement of the heterojunction solar cells in the I–V characteristics and open circuit voltages was achieved in comparison with solar cells on nanowire arrays prepared with similar methods [4,8]. By choosing special measurement conditions in electron beam induced current (EBIC) technique, the functionality of the device was verified and visualized.

2. Method

SiNW arrays were prepared following the method described by Peng et al. [13], i.e., using AgNO$_3$ (0.02 M) and HF (5 M) at room temperature. An n-type (111) Si wafer with a doping concentration of $\sim 1 \times 10^{15}$ cm^{-3} was cleaned by acetone and 2-propanol, and then it was put into H$_2$SO$_4$ (97%) and H$_2$O$_2$ (30%) solution (1:1 by volume) at 80 °C for about 10 min to remove any organic and inorganic contaminations at the surface. The cleaned wafer was mounted on an etching cell, which allows only the polished side to get in contact with the etching solution. A mixture of 10 ml AgNO$_3$ (0.02 M) and 10 ml HF (5 M) was added to the etching cell. Etching was stopped after 30 min, and the sample was rinsed thoroughly with deionised water afterwards.

The cleaning procedure begins with a 3 min dipping in concentrated HNO$_3$ (65%) to remove the large amount silver dendrites on the sample surface. After that, the sample was rinsed in deionised water several times, and then 10 ml aqueous ammonia (NH$_3$) in form of NH$_4$OH (4.6%) together with 5 ml 2-propanol was added to the etching cell. Air was bubbled through the mixture for 25 min. The oxygen in the air increases the ionization of the Ag particles, and the 2-propanol serves as a surfactant to reduce the surface tension allowing the etchant to penetrate into the space or holes between the nanowires, in order to remove the silver particles at the bottom of the nanowires. NH$_4$OH reacts with the Ag to form a soluble complex, and is subsequently released from the surface. The following reactions occur

$$2Ag^+ (aq)+2NH_3 (aq)+H_2O (l) \rightarrow Ag_2O (s)+2NH_4^+(aq)$$

$$Ag_2O (s)+4NH_3 (aq)+H_2O (l) \rightarrow 2[Ag(NH_3)_2]^+ (aq)+2OH^- (aq)$$

It should be noted that prolonged treatment in the NH$_4$OH solution could result in removal of the nanowire layer, as silicon dissolution in alkaline solutions [18–20] is well known. In a further silver removal step the sample was treated by a neutral Na$_2$S$_2$O$_3$ (0.1 M):2-propanol solution for 20 min. The 2-propanol works as a surfactant as well, and silver forms a soluble complex with the thiosulfate S$_2$O$_3^{2-}$ according to the following reaction

$$Ag^+ (aq)+2S_2O_3^{2-} (aq) \rightarrow Ag(S_2O_3)_2^{3-} (aq)$$
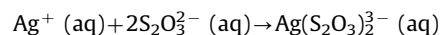
After the cleaning, the sample was dipped into a HF (2%): 2-propanol solution for 8 min to remove the oxide layer on the SiNW surface. The 2-propanol serves again as a surfactant to reduce the surface tension so that the etchant can penetrate the nanowire array to remove the oxide around the NWs completely. It is necessary in this step to use a surfactant, because when the oxide on the tips of the nanowire arrays is removed, the surface on the tips of the nanowires turns from hydrophilic into hydrophobic. Therefore, the HF will not go further into the bottom of the SiNW arrays without using surfactant. After rinsing in deionised water, the sample was immediately placed into the PECVD chamber to deposit the a-Si layer. The deposition was performed at 225 °C. A thin intrinsic a-Si (20 s at a silane flow rate of 2 sccm, chamber pressure of 0.5 mbar) was deposited prior to a highly doped p-type a-Si (2 min. at a silane flow rate of 2 sccm and diborane of 1 sccm (2% diluted in He), respectively, chamber pressure 0.5 mbar). The intrinsic a-Si is very effective in reducing the surface recombination at the interface of a-Si/c-Si [15,21,22]. As transparent conductive oxide (TCO) layer, a $\sim$200 nm polycrystalline Aluminum doped Zinc oxide (AZO) layer was deposited on top of the a-Si layer at a substrate temperature of 225 °C by atomic layer deposition (ALD).

The sample was mesa-etched and the contact areas of the solar cells were determined by a microscope. Finally, the ohmic back side contact was made by rubbing InGa alloy onto the rear side of the wafer.