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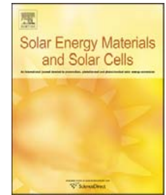

Dry fabrication process for heterojunction solar cells through in-situ plasma cleaning and passivation

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ABSTRACT

We have studied low temperature plasma processes ($T_{sub} \leq 200\,^{\circ}C$) for the efficient cleaning and passivation of c-Si wafers, aiming for fully dry fabrication of heterojunction solar cells. We have experimented with H_2–SiF_4 plasmas in a standard RF PECVD reactor in order to etch the native oxide from the c-Si wafer and a thin a-Si:H layer was deposited from SiH_4 to passivate the c-Si surface. In-situ ellipsometry was used to optimize the process conditions for an efficient surface cleaning. Various plasma treatments were performed before a-Si:H deposition in order to reduce the surface recombination. Optimized process conditions resulted in high effective lifetime values ($\tau_{eff} \approx 1.55$ ms), low effective surface recombination velocities ($S_{eff} \leq 9$ cm s^{-1}) and high implicit open circuit voltages ($V_{oc} \approx 0.713$ V).

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1. Introduction

Crystalline silicon solar cells are a mature technology that currently represents about 90% of the photovoltaic market [1]. The main reason is their high efficiency (PERL structures based on c-Si have demonstrated efficiencies close to 25% [2]), which is not achieved at the moment with lower cost thin film technologies. This has driven continuous research efforts to further increase efficiency while reducing production costs. In this respect, heterojunction solar cells are a promising approach as they allow high efficiencies even for very thin wafers $\sim$100 μm [3]. Moreover, new processes for plasma texturing in order to improve the light trapping on the silicon surface [4], and efforts towards producing ultra-thin silicon substrates ($\leq$50 μm thick) [5], will make c-Si PV technology the dominant one for at least the next ten years.

Wet chemical etching is routinely used by the PV and semiconductor industries for cleaning the silicon wafer surface [6–10]. Solutions based on hydrofluoric acid (HF) and deionized (DI) water are widely used to remove native SiO_2. For high efficiency solar cells, new wet cleaning processes have been developed based on several steps, including RCA cleaning, HF dip and NH_4F for H termination of the c-Si surface [11]. However, the relatively high amount of DI water and chemicals employed in these processes represent an environmental and a financial issue.

In this work, we have systematically studied low damage dry etching to remove the native SiO_2 from c-Si surface using H_2 and SiF_4 gas mixtures in a standard RF PECVD reactor. In-situ UV–vis ellipsometry was used to control and optimize the SiO_2 etching process. Moreover, surface passivation was achieved by depositing a-Si:H immediately after removing the native SiO_2, without breaking the vacuum. We also studied different plasma treatments before the a-Si:H deposition in order to improve the quality of the surface passivation.

2. Experiments

The system used for plasma cleaning is a standard capacitively coupled RF glow discharge PECVD reactor. H_2 and SiF_4 gas mixtures have been used to etch SiO_2 from the surface of c-Si wafers. A real-time UV–vis ellipsometer (Jobin Yvon—MWR UVISEL UV/vis) was used to monitor the native SiO_2 etching during the plasma exposure.

Here we present optimized process conditions for efficient wafer cleaning based on preliminary studies of the effects of pressure and RF power. The most efficient plasma process conditions were found to be an RF power of 10 W and a pressure of 30 mTorr. For these optimized conditions we studied the effect of the gas flow ratio (SiF_4/H_2=0.5, 1, 2, 4 and pure SiF_4).

In order to look for a dependence of the etching process on the substrate doping and process temperature, we used 4 different c-Si wafers: (1) CZ ⟨1 0 0⟩ p type 14–22 Ω cm, (2) FZ ⟨1 0 0⟩ p type 5–10 Ω cm,, (3) FZ ⟨1 0 0⟩ n type 1–5 Ω cm and (4) FZ

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⟨1 1 1⟩ n type 1–5 Ω cm, and two substrate temperatures: 150 and 200 °C.

For passivation studies we used ⟨1 0 0⟩ n type 1–5 Ω cm 280 μm thick double side polished FZ c-Si wafers, upon which 40 nm of a-Si:H was deposited from pure SiH_4 after removing the native SiO_2, without breaking the vacuum. Various plasma treatments were also applied on the crystalline silicon wafer between the plasma cleaning and a-Si:H deposition in order to improve the quality of the passivation. The different treatments consisted on the deposition of an epitaxial layer of 40 nm, an Ar plasma or a H_2 plasma. Table 1 part A (process conditions) summarizes the different processes.

The photoconductance decay technique was used to determine the effective lifetime (τ_{eff}) employing a commercial set-up (Sinton WTC-120). The sample was illuminated with a flash lamp in order to generate excess carriers in the c-Si substrate, which creates a change in the conductivity of the wafer. The dependence of τ_{eff} on the excess carrier density ($\Delta n = \Delta p$) is then measured, and the implicit V_{oc} at 1 sun illumination is deduced [12].

In order to calculate the effective surface recombination (S_{eff}), we use the Eq. (1) where W is the wafer thickness [12–14]. If we assume a high value of the bulk lifetime, then all the recombination occurs on the c-Si surfaces, and the first term of the right side in Eq. (1) can be neglected. Thus an upper limit of S_{eff} is deduced using the Eq. (2):

$$1/\tau_{eff} = 1/\tau_{bulk} + 2S_{eff}/W \quad (1)$$

$$S_{eff} \leq W/(2\tau_{eff}) \quad (2)$$

3. Results and discussion

The imaginary part of the pseudo-dielectric function (Im[ε]) of c-Si was measured by UV–vis ellipsometry, in the energy range of 1.5–4.5 eV. In particular, we carefully monitored the value of (Im[ε]) at 4.2 eV, where the E_2 peak is located, and whose amplitude is related to the c-Si surface quality and to the presence of native SiO_2 on the Si surface [15,16]. This is clearly seen on the inset of Fig. 1 where we plot (Im[ε]) for a c-Si wafer with its native oxide and (Im[ε]) of the same wafer right after a HF dip to remove the native oxide. When the c-Si surface is free of native SiO_2, the amplitude of E_2 is 45, but it decreases to $E_2 \approx 37$ when a thin native oxide layer is present.

Fig. 1 shows the value of E_2 after 5 min of plasma exposure at various SiF_4/H_2 ratios. We can see that the amplitude of E_2 increases with the value of the SiF_4/H_2 ratio and is the highest in the case of a pure SiF_4 plasma. From those results we conclude that a SiF_4 plasma is a more efficient process to etch native SiO_2 than a similar process using a mixture of both gases.

Fig. 2 shows the amplitude of E_2 as a function of SiF_4 plasma exposure time on 4 different substrates, and for two substrate temperatures (150 and 200 °C). In these processes we observe that at the beginning of plasma exposure, the amplitude of E_2 decreases, since at this stage the plasma creates roughness as the SiO_2 is etched away from the c-Si surface. However, after certain plasma exposure time, the E_2 amplitude increases and reaches a maximum, which is related to the complete removal of SiO_2. For longer plasma exposure times, the E_2 peak decreases as a result of the roughening of the c-Si surface induced by the etching of c-Si by the SiF_4 plasma.

In Fig. 2 we observe that the time needed for the amplitude of E_2 to reach a maximum depends on the substrate temperature. At 200 °C the optimum etching time was around 300 s for the four types of c-Si substrates, while at 150 °C the optimum etching time increased to around 380 s. However there is no marked dependence of the etching time on the c-Si doping type or orientation. Note that when SiO_2 is etched at 200 °C the E_2 amplitude is higher than when the process is performed at 150 °C, suggesting a better surface quality. From these studies, we have defined optimal process conditions and plasma exposure times for the effective cleaning of c-Si wafers.

We studied c-Si passivation in order to characterize the quality of the c-Si wafer surface cleaned by plasma. As a reference, we deposited a 40 nm thick a-Si:H passivating layer on both sides of a c-Si wafer after cleaning with a standard HF solution (5% in DI water). This resulted in a τ_{eff} of 1.75 ms as is shown in Table 1.

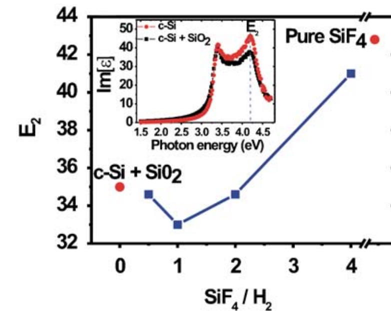

Fig. 1. Effect of SiF_4/H_2 ratio on intensity of E_2 peak measured in-situ, after 5 min of plasma exposure. The insert shows a comparison of two Im[ε] spectrums of c-Si surfaces: one with native oxide and the other measured on the same substrate after removing the native oxide using an HF dip.

Table 1
Native SiO_2 etching process conditions and results of the c-Si passivations.

(A) SiO_2 etching process conditions						(B) Results from passivation			
Process number	T_{sub} (°C)	SiO_2 plasma etching using SiF_4		Plasma treatment before 40 nm of a-Si:H deposition		Lifetime before annealing (ms)	Lifetime after annealing at 200 °C (ms)	Implied V_{oc} (V)	Surface recombination velocity (cm s^{-1})
		Power (W)	Time (s)	Gas	Time (s)				
M0801105. Reference (HF)	150	No	No	No	No	1.71	1.75	0.722	8
M090205	200	10	300	No	No	0.017	0.014	0.551	1000
M090205-2	150	10	380	No	No	0.090	0.219	0.634	63
M090206-1	150	10	380	Epitaxy	360	0.020	0.020	0.562	682
M090209-1	150	10	380	Ar	60	0.018	0.031	0.624	444
M0902010-2	150	10	380	Ar	30	0.118	0.163	0.648	85
M0902010-1	150	10	380	H2	60	0.899	0.961	0.694	14.5
M090316-2	150	10	380	H2	30	1.13	1.23	0.701	12.4
M090212-1	150	5	380	H2	30	1.51	1.55	0.716	9

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