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Interface trap characterization of Al_2O_3/GaN vertical-type MOS capacitors on GaN substrate with surface treatments

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ABSTRACT

We report on the interface trap properties Al_2O_3/GaN vertical-type metal-oxide-semiconductor (MOS) capacitors homogeneously grown on GaN substrates with different surface treatments. The electrical and microstructure characteristics are analyzed with regard to the behaviors and natures of different trap states at and close to the MOS interface. It is shown that only acid cleaning could not effectively suppress the interface traps, while a following $(NH_4)_2S$ passivation drastically reduce the interface state density to the detection limit of ~10^{11} $cm^{-2}eV^{-1}$. At the same time, border traps and fixed charges located close to the MOS interface are also suppressed, leading to a neglecting electrical hysteresis and frequency dispersion in the capacitance-voltage measurement.

1. Introduction

III-V nitride semiconductors are becoming the promising choices for the next-generation high power switching systems owing to their intrinsic large breakdown electric field, high electron saturation velocity, superior chemical and physical stability [1–4]. Recently, with significant progresses in the free-standing GaN substrates, the vertical-type GaN-on-GaN power devices are offering more and more advantages than the lateral AlGaN/GaN high electron mobility transistors (HEMTs) on foreign substrates [5,6]. For example, the lower dislocation density and strain-free epitaxial layer grown on GaN substrate can greatly improve the thermal conductivity and device reliability. In vertical-type GaN power devices, the on-state current flows through the homoepitaxial layer, therefore the issues in the AlGaN/GaN HEMTs such as current-collapse, dynamic on-resistance and inability to support avalanche breakdown can be avoided. Up to now, rapid progress has been achieved in the vertical-type metal-insulator (oxide)-semiconductor (MIS or MOS) field effect transistors (FETs) [7]. However, the quality of the MOS interface strongly affects the electrical properties of the devices. The threshold voltage is much lower and the on-resistance is still higher than the expected values due to the insufficient control of the GaN surface potential [8]. To ultimately improve the performance of GaN-on-GaN vertical MOSFETs and realize real applications, a high-quality and stable MIS/MOS interface with low-density trap states both at and close to the interface is required.

Different insulators such as Al_2O_3, SiO_2, SiN_x or their integrated composite structures have been utilized in the GaN MIS devices especially for the lateral structure. Among them, Al_2O_3 is considered as a better gate insulator benefitting from its high permittivity (8–10), wide band gap (7–9 eV), high breakdown field (10 MV/cm), and favorable conduction/valence band offsets to GaN [6,9]. Typically, Al_2O_3 gate insulator is prepared by atomic layer deposition

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(ALD) due to its precise control in thickness, and pinhole-free characteristics. In principle, a pre-treatment is required to remove the poor-quality native oxidized layer (GaO_x) or carbon impurities, which usually bring high-density interface states ($>10^{13}$ $cm^{-2}eV^{-1}$) by the incomplete chemical bonds or impurities [10,11]. A lot of surface treatments have been attempted to modify the GaN surface grown on sapphire. Usually, acid cleaning could remove the native oxidized layer, however, on the other hand, it will affect the ALD-Al_2O_3 nucleation and bring out large-density traps at the transition layer or inside the Al_2O_3 [6], resulting in a threshold voltage instability [12,13]. Therefore, a following surface passivation/modification or post-treatments are also required. Nevertheless, there is no systematic investigation on the effects of surface treatment/modification to the behaviors of trap states at the Al_2O_3/GaN MOS interface grown on GaN substrate.

In this paper, we systematically analyzed the characteristics of various trap states located not only at but also close to the Al_2O_3/GaN interface at the vertical-type MOS capacitors on GaN substrate with different surface treatments by electrical and microstructure measurements. It is found that, the interfacial discontinuous layer was suppressed by the surface treatments. Simple acid cleaning slightly increased the interface state density, while a following $(NH_4)_2S$ passivation lead to a drastic reduction of interface states and interface border traps. The other interface traps located at the transition layer and/or inside Al_2O_3 dielectric were also analyzed with regard to the electrical and microstructural measurement.

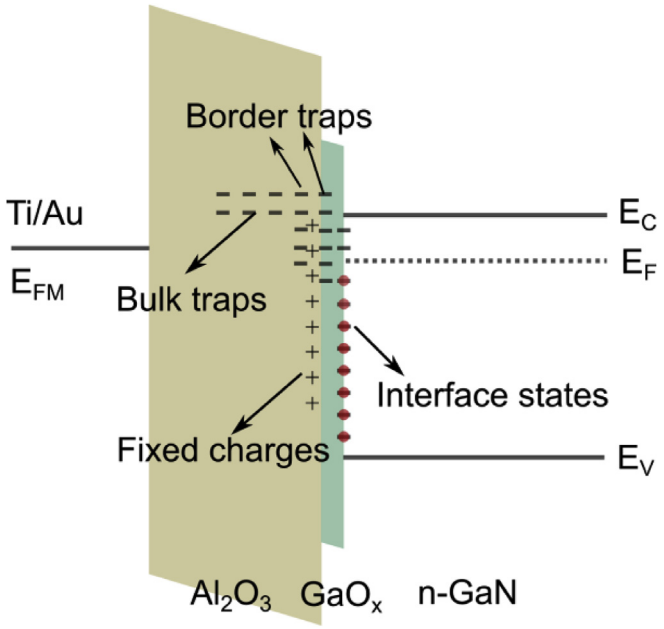

Fig. 1. Schematic band diagram of Al_2O_3/GaN MOS structure, in which the different locations of interface traps are illustrated. The interface states are at the GaN/oxide interface. Border traps refer to the trapping states near the GaN/oxide interface, either in the native GaO_x layer or re-oxidation in the transition region during ALD process. Bulk traps are formed inside the Al_2O_3, but far from the interface. The positive fixed charges in Al_2O_3 are also observed, whose position can be distinguished by related physics model, discussed in the manuscript.

2. Experimental methods

The GaN epitaxial layers with the thickness of 4 μm were grown on free-standing GaN substrates by using a metal-organic chemical vapor deposition system. The growth details can be found in our previous paper [4]. The free electron concentration of the GaN epilayer was estimated to be 1×10^{17} cm^{-3}, which is determined by a *C–V* characterization. The MOS capacitors with ALD-Al_2O_3 dielectric layer used for the interface analysis were fabricated by standard semiconductor device process. Prior to ALD deposition, the GaN epitaxial layer was sequentially cleaned with acetone, methanol, and deionized (DI) water. Then, different treatments were performed to the GaN surface: (a) without any treatment; (b) diluted hydrofluoric acid (HF:H_2O (1:5)) for 3 min at room temperature (RT); (c) HF:H_2O (1:5) for 3 min at RT, followed by ammonium sulfide ($(NH_4)_2S$:H_2O (1:5)) solution for 30 min at 70 °C (two-step treatment). After treatments, the samples were immediately loaded into an ALD chamber for the Al_2O_3 deposition (PICOSUN, SUNALE R-100B). In this process, DI water vapor and trimethylaluminum (TMA) were introduced in an alternating mode, acted as oxidant and metal precursor, respectively. The pulse and purge time for both precursors were 0.1 and 4.0 s, respectively. All Al_2O_3 gate insulators were deposited at 300 °C and the thickness were varied from 10, 20–30 nm. Circular Ni/Au bilayer were E-beam evaporated as the Schottky contacts, patterned via LASER photolithography using a conventional lift-off process. Finally, the Ti/Au Ohmic contacts, was deposited on the backside of GaN substrates by sputtering deposition. The electrical characteristics were performed by capacitance-voltage (*C–V*) measurements using an Agilent 4284A LCR meter. The interface microstructure of Al_2O_3/GaN was obtained through high-resolution transmission electron microscopy (HR-TEM) (JEOL, JEM-2100).

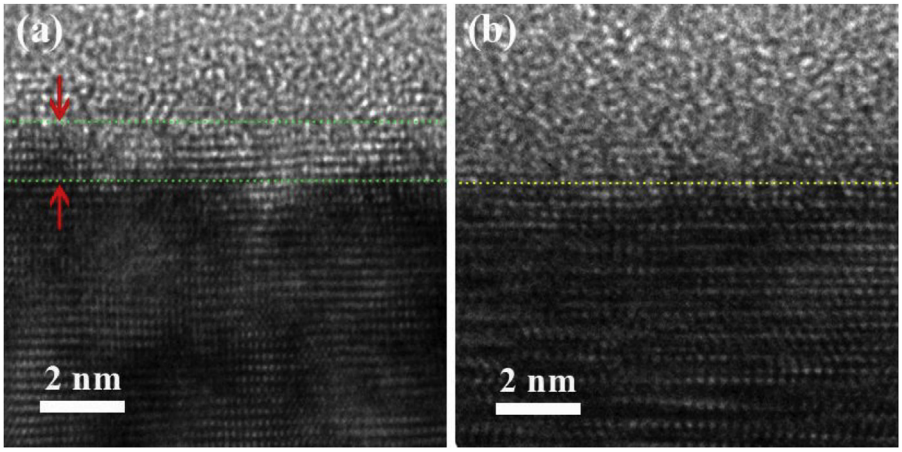

Fig. 2. High-resolution TEM images for ALD-Al_2O_3/GaN interface (a) without any treatment, and (b) with aqueous HF etching + $(NH_4)_2S$ passivation.