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High-performance GaN-based light emitting diodes grown on 8-inch Si substrate by using a combined low-temperature and high-temperature-grown AlN buffer layer

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ABSTRACT

A combined buffer layer growth process was developed to grow crack-free GaN layers on 8-inch Si(111) wafers and so light-emitting diodes (LEDs). The combined buffer layer consisted of 2 nm-thick low-temperature (LT, 850 °C)-AlN, 8 nm-thick graded-temperature AlN, and 200 nm-thick high-temperature (HT, 1100 °C)-AlN layers. The X-ray diffraction (XRD) results showed that the LT-HT-AlN buffer layer exhibited better crystal quality than the HT-AlN buffer layer. The atomic force microscopy (AFM) images revealed that compared to the LT-HT-AlN buffer layer, the HT-AlN buffer layer had a rough surface with numerous bright spots, which correspond to N-polar AlN hillocks. Scanning electron microscopy (SEM) results showed many pits in the HT-AlN buffer layer. Transmission electron microscopy (TEM) results showed that the HT-AlN buffer layer contained about 1.3 nm-thick amorphous Si_xN_y layer at the interface, while the LT-HT-AlN buffer layer showed a relatively smooth interface. It was further shown that using the LT-HT-AlN buffer layer, high-quality crack-free *n*-GaN layers (2.5 μm-thick) were grown on the 8-inch Si(111) substrate, which was confirmed by the XRD and cathodoluminescence results. Subsequently, packaged vertical LEDs (chip size: 1400 × 1400 μm^2) grown on the LT-HT-AlN buffer layers showed higher light output power and chip yield than LEDs with the HT-AlN buffer layer.

1. Introduction

Reduction of the manufacturing cost of GaN-based light-emitting diodes (LEDs) is of a significantly important industrial issue, because they are broadly used as a light source in a wide variety of applications, such as general illumination, displays, automotive headlamp, and medical devices [1–4]. Commercial GaN-based LEDs are mainly grown on sapphire and SiC substrates. However, to cut down their manufacturing costs, Si substrates have been employed as a promising alternative to their competing counterpart because of their low cost, wafer size scalability and matured semiconductor fabrication processes [5]. In spite of these merits, the use of Si substrates for the growth of GaN encounters several technical problems remained to be solved. First, there is a large lattice constant mismatch between GaN and Si (−17%) [6], resulting in a high density of dislocations and resultant low internal quantum efficiency (IQE). Second, there is a large mismatch in thermal expansion coefficient (~56%) between GaN and the Si substrate [7]. This causes the building up of significant tensile stress in the GaN when the wafer cools down from the growth temperature, which results in the generation of crack or serious wafer bowing. The other issue is related to the meltback etching of Si wafer [8], taking place because of the reaction between Si and Ga. Therefore, to minimize these negative effects and so to grow high-quality GaN, researchers have proposed a variety of different methods, including Al(Ga)N-based interlayers [9,10], epitaxial lateral overgrowth (ELOG) [11], patterned Si substrate [12], graded AlGaN buffer layers [13,14], Al(Ga)N/GaN superlattice layers [15,16], and a nanoporous GaN layer [17]. For example, Lahrèche et al. [7] investigated the effect of high-temperature (HT) (950–1150 °C)-grown AlN interlayers on the crystallinity of GaN layers grown on Si(111) substrates by low-

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pressure metalorganic vapour-phase epitaxy (LPMOVPE) and reported that the growth mode of GaN depended on the AlN growth temperature and the best GaN had a full-width at half-maximum (FWHM) of the (0002) X-ray diffraction (XRD) line in rocking curve of about 656 arcsec, a dislocation density of low 10^{10} cm^{-2}, and a surface root-mean-square (RMS) roughness of 0.3 nm. Furthermore, the use of a low-temperature AlN (LT-AlN) layer has been known to be an efficient way of growing crack-free GaN [18–25]. For example, Bläsing et al. [18] investigated how LT (720 °C)-grown AlN (25 nm thick) interlayers affected the growth of thick GaN layers on Si(111) substrates and showed that tensile stress was reduced with decreasing interlayer growth temperature. It was shown that HT-grown AlN interlayers were pseudomorphic, while LT-AlN relaxed the tensile stress. Consequently, GaN layers grown on a LT-AlN interlayer were grown under compressive interlayer-induced strain. Lu et al. [20] investigated the depth distribution of the strain-related tetragonal distortion in the GaN epilayer with LT (600 °C)-AlN interlayer (LT-AlN IL) (8–16 nm thick) on Si(111) substrate by means of Rutherford backscattering and channeling, and reported that the strain compensation effect would occur when the thickness of the LT-AlN IL is beyond a critical thickness (e.g., at least 16 nm). Dadgar et al. [22] investigated the improvement of performance of GaN-based LEDs on 2 in. Si(111) substrates by the low-temperature (720 °C) AlN:Si seed layer (10–15 nm thick) and two low-temperature AlN:Si interlayers and found that the GaN exhibited a FWHM of the (002) XRD line in rocking curve of about 637 arcsec and a dislocation density of ~10^{9} cm^{-2}. Therefore, the LEDs (a wavelength of 455 nm) gave low turn-on voltages of 2.5–2.8 V, a series resistance of 55 Ω, and an output power of 152 μW at a current of 20 mA. Recently, Chen et al. [24] investigated the effect of graded-temperature-grown (1000 °C) AlN buffer layers (with a step of 50–100 °C) on the structural properties of GaN on Si(111) and found that compared to the previously reported buffer growth methods, this graded-temperature technique produced good-crystallinity GaN even with a thinner buffer layer. It was shown that combination of the graded-temperature AlN and an GaN/AlN superlattice interlayer enabled the growth of thick crack-free GaN layers of 3.7 μm in total thickness. Consequently, the quantum well (QW) sample with the highest graded temperature number for depositing the AlN buffer exhibited the weakest quantum-confined Stark effect and the highest internal quantum efficiency (IQE). These results indicate that the crystallinity of the AlN buffer layers plays a crucial role in growing high-quality GaN layers. In this study, we investigated the structural properties of the combined buffer layers consisting of 2 nm-thick LT (850 °C)-AlN, 8 nm-thick graded-temperature AlN, and 200 nm-thick HT-AlN buffer layers and their effect on the crystallinity of GaN on 8-inch Si(111). Subsequently, packaged vertical LEDs grown on 8-inch Si(111) with these buffer layers were fabricated, and the electrical and optical performance of 300 packaged LEDs was characterized.

2. Experimental procedure

A metalorganic chemical vapour deposition (MOCVD) system was used to grow the samples on 8-inch Si(111) substrates. Prior to growth, an *n*-type Si(111) substrate was etched using H_2SO_4: H_2O_2: H_2O (3:1:1) and HF (5%) to remove native oxide and to have Si surface hydrogen-passivated. To investigate the effect of the buffer layers, two types of buffers were grown on the Si(111) substrates. For reference sample, TMAl was first pre-flowed at 850 °C for 10 s on the Si(111) substrate, followed by the growth of 180 nm-thick high-temperature (HT) AlN at 1100 °C. For controlled samples, TMAl was first pre-flowed at 850 °C for 10 s on the Si(111) substrate, followed by the growth of 2 nm-thick low-temperature (LT) AlN at 850 °C. After that, 18 nm-thick AlN was grown while ramping up temperature, followed by the growth of 180 nm-thick HT AlN at 1100 °C. InGaN/GaN-based vertical-geometry LEDs (a wavelength of ~445 nm) were grown on 8 inch Si(111) substrates. The epilayer stacks of the LEDs consisted of LT-HT-buffer layers, a 2.5 μm-thick undoped GaN at 1040 °C under a pressure of 200 Torr, a 2 μm-thick Si-doped *n*-GaN layer ($n_d = 7 \times 10^{18}$ cm^{-3}) at 1040 °C, a twenty pairs of InGaN/GaN (2 nm/2 nm) superlattice strain layer, active region of five pairs of InGaN/GaN (3 nm/6 nm) multi-quantum wells (MQWs) at 760 °C under a pressure of 200 Torr, a 20 nm-thick Mg-doped $Al_{0.15}Ga_{0.85}N$ electron blocking layer and an 80 nm-thick Mg-doped *p*-GaN layer at 960 °C. For comparison, reference LEDs were also grown with the HT AlN buffer layer. The *p*-GaN was *in-situ* activated at 700 °C for 5 min in a N_2 stream within the MOCVD chamber. Detailed fabrication processes of vertical LEDs (1400×1400 μm^2) were published elsewhere [26]. As a *p*-reflector, a Ag layer was deposited by radio frequency (RF)-magnetron sputtering. A bonding metal alloy, consisting of Au, Sn, and Cu, was then deposited on the reflector by a dual e-beam system. After completing the LED structures, the whole wafer (8 inch) was bonded to the Si wafer by thermal compression at 300 °C. A chemical lift-off (CLL) process was then performed using an acid solution to remove the Si substrate. After chip isolation etching, N-polar *n*-GaN was textured by etching with a KOH solution at 40 °C, followed by the e-beam evaporation *n*-Ohmic electrode (100 nm Ti/200 nm Ni/2 μm Au). To investigate the electrical, optical, and structural characteristics, the wafer-level LED samples were cut into chips and encapsulated into standard LED lamps. Blue LED chips were packaged (5630 size PKG) and characterized at room temperature. For the characterization of LED chips, current-voltage (*I*–*V*) characteristics were examined using an Agilent B1505A system. The light output power-drive current relations were measured using an integrating sphere (Instrument Systems GmbH. ISP 500) with Spectroscope (CAS 140CT) and Sourcemeter (Keithley KE2601A). Raman scattering was used to characterize the stain state of GaN layers and transmission electron microscopy (TEM) and cathodoluminescence (CL) examinations were performed to study the microstructures and defects. Atomic force microscopy (AFM) was used to characterize the surfaces of epilayers. The crystalline quality was characterized with X-ray diffraction (XRD) rocking curve measurements (ω scans). A wafer inspection system (Zootos Co., Korea) was used to characterize the 8-inch wafer, which automatically detected specific objects, such as cracks and particles by acquiring a digital image using a microscope. The performance and production yields of vertical LEDs were carried out with a chip probing system (QMC LEP-200™).

3. Results and discussion

The crystallinity of the AlN buffer layers was characterized by X-ray diffraction (XRD) in ω rocking curve scan of the (0002) line of AlN. The XRD results show that the HT-AlN buffer layer has a full-width at half-maximum (FWHM) of 1400 arcsec, whereas LT-HT-AlN buffer layer has a FWHM of 789 arcsec. This indicates that the introduction of 10-nm-thick LT and graded-temperature AlN is effective in improving the crystallinity of AlN, consequently resulting in the improved GaN, as will be described later. Fig. 1 exhibits AFM images (scan area: 5×5 μm^2) obtained from the HT-AlN and LT-HT-AlN buffer layers. The HT-AlN buffer layer shows numerous bright spots, which correspond to N-polar AlN hillocks [27], while the LT-HT-AlN buffer layer reveals only few bright spots. The HT-AlN buffer layer reveals a rough surface with a root-mean-square (RMS) roughness of 2.5 nm. On the other hand, the surface of the LT-GT-AlN buffer layer is fairly smooth with an RMS