



Modulation of interfacial and electrical properties of ALD-derived HfAlO/Al₂O₃/Si gate stack by annealing temperature



J. Gao ^{a,b}, G. He ^{a,*}, M. Liu ^{c,**}, J.G. Lv ^{d,***}, Z.Q. Sun ^a, C.Y. Zheng ^a, P. Jin ^a, D.Q. Xiao ^a, X.S. Chen ^e

^a School of Physics and Materials Science, Radiation Detection Materials & Devices Lab, Anhui University, Hefei 230601, China

^b School of Sciences, Anhui University of Science and Technology, Huainan 232001, China

^c Key Laboratory of Materials Physics, Anhui Key Laboratory of Nanomaterials and Nanostructure, Institute of Solid State Physics, Chinese Academy of Sciences, Hefei 230031, China

^d Department of Physics and Electronic Engineering, Hefei Normal University, Hefei 230061, China

^e National Laboratory for Infrared Physics, Chinese Academy of Sciences, Shanghai Institute of Technical Physics, 500 Yutian Road, Shanghai 200083, China

ARTICLE INFO

Article history:

Received 10 November 2015

Received in revised form

2 August 2016

Accepted 27 August 2016

Available online 29 August 2016

Keywords:

High-k dielectric

Interface thermal stability

Atomic-layer-deposition

Band alignment

Electrical properties

Leakage current mechanism

ABSTRACT

In current work, effects of rapid thermal annealing on the interface chemical bonding states, band alignment, and electrical properties of atomic-layer-deposition-derived HfAlO/Al₂O₃ gate stack on Si substrates have been studied by X-ray photoemission spectroscopy (XPS), UV–Vis transmission spectroscopy, and electrical measurements. XPS analyses have shown that HfAlO alloy and mixed silicate (Hf–Al–O–Si) increase after post-deposition annealing process. By means of UV–Vis transmission spectroscopy measurements, reduction in band gap for 400 °C-annealed sample has been observed. Accordingly, reduction in the valence band offset and increase in the conduction band offset have been detected for HfAlO/Al₂O₃/Si gate stack annealed at 400 °C. Various current conduction mechanisms, such as Poole–Frenkel emission, Fowler–Nordheim (FN) tunneling, and space-charge-limited (SCL) conduction, have been analyzed. Detailed electrical measurements reveal that current conduct mechanisms is SCL conduction at lower field region and FN tunneling and SCL conduction are dominant conduction mechanism at higher field region.

© 2016 Elsevier B.V. All rights reserved.

1. Introduction

In order to meet the requirements of continuous down-scaling of complementary metal oxide semiconductor (CMOS), many alternative high-k gate dielectric materials have been widely employed and investigated [1,2]. Due to a combination of outstanding structure and good electrical properties, HfO₂ have been paid more attention as alternative insulator for MOS application [3–5]. Moreover, additional elements, for instance, Si, Al, Zr, Ti, and La can be incorporated into hafnium oxide to improve the thermal stability, for instance, suppressing crystallization temperature [6–8]. Among the hafnium-based high-k oxide, HfAlO has

* Corresponding author.

** Corresponding author.

*** Corresponding author.

E-mail addresses: ganghe01@issp.ac.cn (G. He), mliu@issp.ac.cn (M. Liu), jglv@htc.edu.cn (J.G. Lv).

been extensively studied due to its high crystallization temperature up to 900 °C, large band gap, and improved thermal stability [9,10]. However, incorporation of Al₂O₃ is not helpful in blocking the oxygen, which brings out unnecessary interface layer and causes severe degradation of device performance [8]. Considering that Al₂O₃ has superior interface stability, this make it suitable as diffusion barrier between hafnium-based oxide and Si in CMOS processing. It was found that about 1 nm thickness of Al₂O₃ buffer layer can effectively suppresses the Si diffusion into HfO₂, suppresses the formation of Hf-silicates or Hf-silicides at Si interface, and leads to an optimal silicon oxide/Si interface during annealing up to 800 °C [11]. The Al₂O₃ buffer layer can effectively improves the interfacial and electrical characteristics [11–13]. Nowadays, considerable works controlled diffusion of Si into high-k material using Al₂O₃ buffer layer during [11–13]. However, few researchers achieved the systematic studies of rapid thermal annealing temperature dependence of interfacial and electrical properties of HfAlO with Al₂O₃ diffusion barrier layer.

In current work, 1.2 nm thickness of Al₂O₃ buffer layer has been

introduced to suppresses the Si diffusion. Post-deposition annealing effects on interfacial, electrical properties, and leakage current mechanism for atomic layer deposited HfAlO/ Al_2O_3 /Si gate stacks has been investigated systematically. Post-deposition annealing was carried out under high vacuum ambient condition after HfAlO/ Al_2O_3 gate stack were deposited by atomic layer deposition. *Ex-situ* x-ray photoelectron spectroscopy (XPS) measurements was conducted to investigate the interfacial properties of HfAlO/ Al_2O_3 /Si gate stacks. To explore the electrical properties of ALD-derived HfAlO/ Al_2O_3 /Si gate stacks, a set of Al/HfAlO/ Al_2O_3 /n-Si/Al MOS capacitors were fabricated. Based on the measurements of capacitance–voltage (*C–V*) and current density–voltage (*J–V*), electrical parameters and the leakage current mechanisms of MOS capacitors have been systematically discussed.

2. Experimental details

N-type (100) Si wafers with carrier concentration of $1 \times 10^{15} \text{ cm}^{-3}$ and resistivity of 1–10 $\Omega \text{ cm}$ were subjected to modified RAC cleaning. Then, the Si substrates were dipped into a diluted hydrofluoric (HF) solution for 1 min to remove the native oxide of SiO_2 , rinsed with deionized water and then blown dry with nitrogen. After that, samples were loaded into ALD chamber for deposition immediately. Prior to the dielectrics deposition, ultra-thin Al_2O_3 layer of 1.2 nm with growth rate of 0.12 nm/cycle was deposited as interface control layer on the as-cleaned Si substrates by ALD, followed by the deposition of the HfAlO dielectric layer of 21.0 nm in the same condition. The Al_2O_3 incorporation in HfO_2 is achieved by growing HfO_2 and Al_2O_3 alternately, that two cycles ALD layers of HfO_2 and following one cycle ALD layers of Al_2O_3 , and then, this sequence is repeated *n* times to achieve the desired 21.0 nm thickness, by using the model of $[2\text{Hf} + 1\text{Al}] \times n$. The metal precursors for Al and Hf were trimethylaluminum (TMA) and tetrakis (ethylmethylamino) hafnium (TEMAH), respectively. And deionized water acted as the oxygen source. The Hf precursor was heated to 75 °C, while H_2O and Al precursor were set at room temperature. The precursors were alternately introduced to the reactor chamber using high purity N_2 as carrier gas. The time of one Al_2O_3 cycle was composed of 0.02 s TMA pulse, 8 s N_2 purge, 0.02 s H_2O pulse, and 8 s N_2 purge. And the typical ALD growth cycle for HfO_2 was 0.15 s TEMAH pulse/25 s N_2 purge/0.02 s H_2O pulse/25 s N_2 purge. The growth temperature and base pressure in the ALD chamber were 200 °C and 0.2 Torr, respectively. The atomic ratio of Hf: Al in the HfAlO films is about 0.52: 0.48 evaluated by energy dispersive spectroscopy (EDS). Considering the precursor ratio (TEMAH: TMA) of 2:1, it can be concluded that the evaluated stoichiometry coefficients are in accordance with theoretical calculations (the atomic ratio of Hf: Al in the HfAlO films is 1:1). After deposition, rapid thermal annealing (RTA) process was performed at 400, 500 and 700 °C for 60s in a vacuum of 6.3×10^{-5} bar, respectively. In order to evaluate the electrical characteristics of the dielectric layers, Al/HfAlO/ Al_2O_3 /Si/Al MOS capacitors were fabricated by direct current (DC) sputtering Al top electrode through a shadow mask with an area of $7.07 \times 10^{-4} \text{ cm}^2$ and the back surfaces of all samples were deposited with Al film by DC sputtering after the back surface oxide stripping to decrease contact resistance.

Ex situ XPS measurements were performed by using (ESCALAB 250Xi) system, equipped with an Al K_α radiation source (1486.6 eV) and hemispherical analyzer with a pass energy of 20 eV. The collected data were corrected for charging effect-induced peak shifts using the binding energy (BE) of C 1s peak of substrate (284.6 eV). Spectral deconvolution was performed by Shirley background subtraction using a Voigt function convoluting the Gaussian and Lorentzian functions. In all the spectra, different color lines show the measured and fitted XPS results, respectively.

About 40 nm thick HfAlO/ Al_2O_3 films were deposited on quartz substrate to obtain their optical band gaps (E_g) by absorbance spectrum using ultraviolet–visible spectrophotometer (Shimadzu, UV-2550) with wavelength ranging from 190 to 900 nm. The thickness of films was measured by using spectroscopic ellipsometry with a commercial instrument (Shanghai Sanco Instrument Co., Ltd., SC630). A semiconductor device analyzer (Agilent B1500A) combined with Cascade Probe Station was used for *C–V* and *I–V* measurement at room temperature. Short circuit and open circuit calibration were performed before real measurements. And the DC voltage was swept from negative to positive or back and forth to perform single and double sweeps at different frequencies (0.5–1 MHz). Additionally, the leakage current properties were measured by B1500A. All the electrical measurements were performed in a dark box.

3. Results and discussion

3.1. XPS characterization

Fig. 1 shows the core level survey spectra of HfAlO/ Al_2O_3 /Si gate stack at a pass energy of 150 eV and a take-off angle of 45°. It can be seen that all characteristic peaks are derived from Hf 4f, Al 2p, O 1s and Si 2p as well as a small amount of C 1s component introduced from thin film growth process or air contamination during measurement. Fig. 2 shows the Si 2p core-level XPS spectra as a function of annealing temperature. As shown in Fig. 2, all of Si 2p core-level spectra are fitted with seven peaks. For the as-deposited sample, the fitted substrate doublet peaks (Si-Si) have a separation of 0.57 eV, which is composed of the Si 2p_{3/2} for 99.27 eV and Si 2p_{1/2} for 99.84 eV. The other peaks are corresponding to Si-O bonds located at 100.29 eV (Si^{1+}), 101.05 eV (Si^{2+}), 101.75 eV (Si^{3+}) and 103.2 eV (Si^{4+}). An additional silicate (Hf-Al-O-Si) peak can be fitted at 102.6 eV, which is 3.03 eV higher than the substrate peak (99.27 eV). This is identical with those reported by Chiam et al. [14]. Similar to the as-deposited film, there are two broad peaks for the annealed films, the peak set at lower binding energy is attributed to Si-Si bonds, another peaks at higher binding energies include Si-O bonds and silicate. It can be seen that for the peak at higher binding energy there is a slight shift to the higher binding energy for the sample annealed at 400 and 500 °C, and a large shift to the higher binding energy for the 700°C-annealed sample. Additionally, with increasing the annealing temperature there is a continuous increase in the intensity ratio of the high binding energy content. From Fig. 2, it can

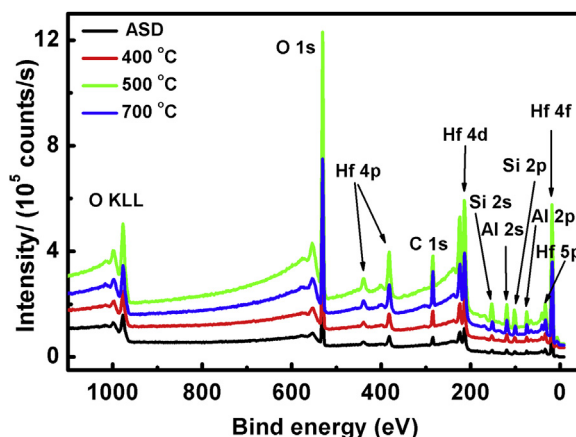


Fig. 1. Core level survey spectra of HfAlO/ Al_2O_3 /Si gate stack as functions of annealing temperature.

Download English Version:

<https://daneshyari.com/en/article/7995388>

Download Persian Version:

<https://daneshyari.com/article/7995388>

[Daneshyari.com](https://daneshyari.com)