



# Controllable nano-texturing of diamond wire sawing polysilicon wafers through low-cost copper catalyzed chemical etching

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## ARTICLE INFO

### Article history:

Received 31 January 2018

Received in revised form 12 March 2018

Accepted 17 March 2018

Available online 17 March 2018

### Keywords:

Semiconductors

Copper-catalyzed chemical etching

Microstructure

Antireflection properties

## ABSTRACT

The depressing texturation and stubborn directional saw marks on diamond wire sawing (DWS) polysilicon wafers has resulted in severe limitations for the mass application of DWS technology in PV market. Herein, a simple and low-cost copper-assisted chemical etching method was presented to controllably nano-texturing DWS polysilicon wafers. The work firstly reveals the adjustment of anion species in copper salts can readily control the nanostructure during the copper-catalyzed etching process. After etching, the obtained inverted pyramid structure can effectively reduce the reflectivity of the silicon wafer surface, the reflectance can be as low as 5.8% in the wavelength range of 300–1100 nm. Moreover, the surface saw marks are removed after etching, and the novel texture method guarantee the low recombination rates. The effective texturing method shows a promising potential application in the photovoltaic field.

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## 1. Introduction

Diamond wire sawing (DWS) technique has the prospect of becoming the next-generation slicing technique for fabricating low-cost Si solar cells, because of its intrinsic advantages, such as higher productivity, lower material loss, higher precision in cutting thin wafer and less surface damages [1]. However, the conventional isotropic texturization system of  $\text{HNO}_3/\text{HF}$  used in multi-wire slurry sawing (MWSS) polysilicon wafers cannot effectively reduce the reflection of DWS wafers [2,3], which has caused that the DWS polysilicon wafers are still unacceptable in the current photovoltaic (PV) industry [4].

Metal-catalyzed chemical etching (MCCE) is considered a potential alternative for texturing DWS polysilicon wafers due to its simple and low-cost [5–7]. However, compared with the gold or silver-assisted silicon etching, the copper-assisted etching in the conventional  $\text{HF}/\text{Cu}(\text{NO}_3)_2$  system is low efficiency [8,9], which is mainly attributed to low redox potential ( $\sim 0.34$  eV) of  $\text{Cu}^{2+}/\text{Cu}$ . Furthermore, copper ions have preferential formation of dense copper film on the Si surface, which will hinder the etching of Si [10]. It has been proved that addition oxidant with higher redox

potential (such as  $\text{H}_2\text{O}_2$  or  $\text{FeCl}_3$ ) in etching system would suppress the formation of dense copper film and improve silicon etching [11].

In this work, a novel copper-assisted chemical etching method was presented to controllably nano-texture DWS polysilicon wafers. The large-scale inverted pyramid arrays with excellent antireflection and saw marks removing ability have been obtained which is crucial to prepare high-efficiency solar cell and reduces photovoltaic (PV) power cost.

## 2. Experimental sections

The p-type DWS polysilicon wafers with thickness of  $200 \pm 20$   $\mu\text{m}$  and resistivity of  $1\text{--}3 \Omega \text{ cm}$  were used, and the wafers were sliced into size of  $30 \times 30 \text{ mm}^2$ . Before etching, the wafers were cleaned in acetone, ethanol and deionized water for 10 min under sonication, respectively. And then the samples were immersed in 10% HF solution for 10 min in order to remove native  $\text{SiO}_2$ . Subsequently, these wafers were put into the etching solution, and the detailed etching parameters were shown in Table 1. After that, samples were immersed in concentrated  $\text{HNO}_3$  solution to eliminate residual Cu-NPs. At last the etched Si wafers were thoroughly rinsed with distilled water and dried under dry nitrogen. The morphologies of as-fabricated samples surfaces were analyzed by

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**Table 1**Etching conditions of DWS multicrystalline silicon wafers by HF/HNO<sub>3</sub> system and Cu-catalyzed chemical etching system.

HF/HNO <sub>3</sub> etching	[HF]/V 20 mL	[HNO <sub>3</sub> ]/V 10 mL	[DI]/V 50 mL	Etching time/min 20	Sample no. Sample 1
Cu-catalyzed etching	[HF]/M 5.6	[H <sub>2</sub> O <sub>2</sub> ]/M 3.0	[CuSO <sub>4</sub> ]/M 0.05	Etching time/min 15	Sample 2
	[HF]/M 5.6	[H <sub>2</sub> O <sub>2</sub> ]/M 3.0	[CuCl <sub>2</sub> ]/M 0.05	Etching time/min 15	Sample 3
	[HF]/M 5.6	[H <sub>2</sub> O <sub>2</sub> ]/M 3.0	[Cu(NO <sub>3</sub> ) <sub>2</sub> ]/M 0.05	Etching time/min 15	Sample 4
	[HF]/M 5.6	[H <sub>2</sub> O <sub>2</sub> ]/M 3.0	[Cu(NO <sub>3</sub> ) <sub>2</sub> ]/M 0.05	Etching time/min 15	Sample 4

scanning electron microscopy (SEM, FEI, USA). The surface reflectivity of wafers was measured by the Ocean Optic USB-4100 fiber spectrometer with an integrating sphere. The  $\mu$ -photoconductance decay function of Semilab WT-2000/2M was used to measure the effective lifetime before and after texturing.

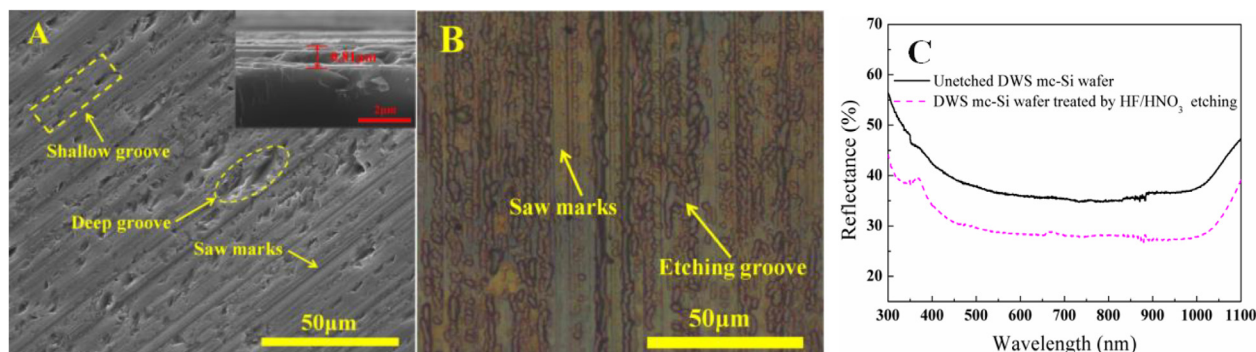
### 3. Result and discussion

Numerous brittle grooves and pits, and parallel plastic saw marks are observed on the as-cut DWS polysilicon wafers surface (as shown in Fig. 1A). According to the previous research [6,7], the smooth saw marks region was covered by amorphous layers, which were caused by the plastic friction during the DWS process. The grooves with depth of 0.1–0.8  $\mu$ m are mainly due to the fragile stripping. After etching in HF/HNO<sub>3</sub> system, some worm-like groove are preferentially formed in brittle damage zone, the smooth plastic region show stubborn anti-etching ability and the saw marks are still observed. As expected, the reflectivity characterizations indicate an awful antireflection ability for isotropic acidic etching.

In order to improve the unsatisfied texturization, the copper-catalyzed chemical etching was introduced to etch the wafer. The morphologies of samples were characterized after etching under the three different etching system. Fig. 2(a) shows that, after the etching under HF/CuSO<sub>4</sub>/H<sub>2</sub>O<sub>2</sub> system, all cutting marks and deep grooves are discovered on the surfaces of sample 2, and numerous ditch-like structures with various lengths are present according the magnified characterization. Fig. 2(b) tells that, with CuCl<sub>2</sub>, the cutting marks are dramatically reduced, at the same time, the uniform, shallow and wormlike pits are formed on the etched wafer surface. It should be noted that the resulting wormlike texturization structure is slightly similar to multi-wire slurry sawing (MWSS) polysilicon wafers endured by HNO<sub>3</sub>/HF etching system. Fig. 2(c) presents that with HF/Cu(NO<sub>3</sub>)<sub>2</sub>/H<sub>2</sub>O<sub>2</sub> etching system, the cutting marks disappear and numerous uniform square holes

structure are observed on DWS polysilicon wafers surface. According to the Fig. 2(d) and (e), the holes have inverted pyramids structure with wide of 1.5–2.5  $\mu$ m and depth of 1.5–3  $\mu$ m. The magnified cross-sectional SEM image reveals that the numerous etching pits were present on inverted pyramid sidewalls, which can be attributed to the copper nanoparticles nucleation and dissolution of silicon sidewall. Although the concentrations of HF, H<sub>2</sub>O<sub>2</sub> and copper ions are same, the anion species in copper salts can affect the deposition and etching behaviors, subsequently control the nanostructure during the etching process [12]. After etching, the surface color of Si wafers turns from steel gray (original wafer) to gray (CuCl<sub>2</sub>), yellowish-brown (CuSO<sub>4</sub>) and black-brown (Cu(NO<sub>3</sub>)<sub>2</sub>), respectively. The reflectance spectra results indicate that different improvement of light trapping have been achieved through copper-assisted texturing treatment under different copper salt system, and one noteworthy phenomenon is that the inverted pyramid structure has presented excellent antireflection ability. The average reflectivity dramatically reduces from 41.8% to 5.8% in the wavelength range of 300 ~ 1100 nm. The excellent antireflection ability of inverted pyramid structure has been confirmed by the previous numerical simulation results [13], which show a promising application potential in the low-cost DWS polysilicon solar cell.

Fig. 3 presents the  $\mu$ -photoconductance decay ( $\mu$ -PCD) lifetime maps of 3 cm  $\times$  3 cm sample. It indicates that without etching, the average effective carrier lifetimes ( $\tau_{\text{eff}}$ ) of naked DWS wafer is 1.20  $\mu$ s, and after the CuSO<sub>4</sub>, CuCl<sub>2</sub> and Cu(NO<sub>3</sub>)<sub>2</sub>-catalyzed texturing, the average carrier lifetime of the textured wafers are 1.312  $\mu$ s, 1.395  $\mu$ s and 1.422  $\mu$ s, respectively. This increasing change trend is similar to the previous texturing process that combines TMAH pre-polishing and routine NaOH texture [3]. Compared with the silver-catalyzed texturization [14], the results in this work demonstrate that the inverted pyramidal structure has an attractive potential to balance both the maximum antireflection and effective carrier lifetimes at the same time.



**Fig. 1.** SEM images of un-etched DWS mc-silicon wafers (A), metallographic micrographs of DWS mc-silicon wafers by HF/HNO<sub>3</sub> etching (B), reflectivity of DWS mc-silicon wafers before and after the HF/HNO<sub>3</sub> etching (C).

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