Materials Letters 182 (2016) 206–209

Contents lists available at ScienceDirect

Materials Letters

journal homepage: www.elsevier.com/locate/matlet

Embedding of copper into submicrometer trenches in a silicon substrate using the molecular precursor solutions with copper nano-powder

Hiroki Nagai [a], Tatsuya Suzuki [b], Takayuki Nakano [c], Mitsunobu Sato [a,*]

[a] Department of Applied Physics, School of Advanced Engineering, Kogakuin University, Japan
[b] Applied Chemistry and Chemical Engineering Program, Graduate School, Kogakuin University, Tokyo, Japan
[c] Department of Electrical and Materials Science, Faculty of Engineering, Shizuoka University, Shizuoka, Japan

ARTICLE INFO

Article history:
Received 10 April 2016
Received in revised form
24 June 2016
Accepted 29 June 2016
Available online 29 June 2016

Keywords:
Molecular precursor method
Trench
Copper
Dip coating
Heat treatment

ABSTRACT

Metallic copper was completely embedded in the trenches (0.2–1.0 μm wide and 5.0 μm deep) by heat-treating a mixed precursor at 350 °C for 30 min under an Ar flow of 1.5 L min^{-1} in a tubular furnace. An ethanol solution containing a dibutylammonium salt of a Cu(II) complex of EDTA ligand, a Cu(II) complex of propylamine, and the Cu nano-powder (20–40 nm) was used to fill the trenches before the heat treatment. Si substrates with the trenches were immersed in this precursor solution under ultrasonic irradiation, and then slowly withdrawn from the solution. The dip coating and heat treatment steps were repeated. The cross-section FE-SEM images of the treated substrate indicate that the embedded copper after two heat treatments of the precursor solution filled the trenches without voids. The XRD pattern of the resulting film on the Si substrate without trenches deposited under identical conditions suggests that the embedded components mainly consisted of copper with Cu_2O as a minor product. Using the four probe method, the electrical resistivity of this resulting film (300 nm thick) was found to be $3.8(5) \times 10^{-5}$ Ω cm.

1. Introduction

Next-generation ultra-large-scale integration (ULSI) circuits will have smaller features with narrower line widths, which necessitates the development of novel techniques for void-free copper filling of submicrometer-wide trenches. The commonly used techniques for filling trenches include physical vapor deposition (PVD), chemical vapor deposition (CVD), and electroplating. Compared to PVD and CVD methods, the electroplating process has the ability to fill submicrometer trenches and via holes in a bottom-up fashion, while avoiding the formation of seams and voids [1,2]. In a typical process, a palladium catalyst is deposited over dielectric layers to initiate the electroless plating on a diffusion barrier layer [3]. However, the obtained palladium particles tend to agglomerate into clusters with sizes typically from tens to hundreds of nm [4–6]. Thus, the size of metal catalyst particles has to be smaller during electroless deposition in narrow trenches for the next-generation ULSI circuits.

We recently reported the fabrication of semi-transparent highly conductive copper thin films well-adhered to a Na-free glass substrate using a solution-based process referred to as molecular precursor method (MPM) [7]. This method is based on the design of metal complexes in coating solutions, which offer many practical advantages such as excellent stability, homogeneity, miscibility, and coatability because the metal complex ions with high stability can be dissolved in suitable solvents such as ethanol after combining with appropriate alkylamines. In this study, metallic copper was successfully embedded in the trenches with widths of 1.0, 0.5, and 0.2 μm and a depth of 5 μm in a Si substrate covered with very thin SiO_2 using the MPM.

2. Experimental

2.1. Preparation of the precursor solutions

A precursor solution (S_A) containing a Cu^{2+} complex of EDTA was prepared according to our previously reported method [8]. Second precursor solution (S_B) containing a Cu^{2+} complex of propylamine was prepared by adding 2.1 g (9.3 mmol) of $(HCOO)_2Cu \cdot 4H_2O$ and 2.2 g (37.2 mmol) of propylamine to 5 g of ethanol followed by 1 h stirring at room temperature. The Cu precursor solution was prepared by mixing 0.8 g of S_A and 5.6 g of S_B in 11.9 g of ethanol under ultrasonic stirring for 30 min. The

* Corresponding author.
E-mail address: lccsato@cc.kogakuin.ac.jp (M. Sato).

http://dx.doi.org/10.1016/j.matlet.2016.06.123
0167-577X/

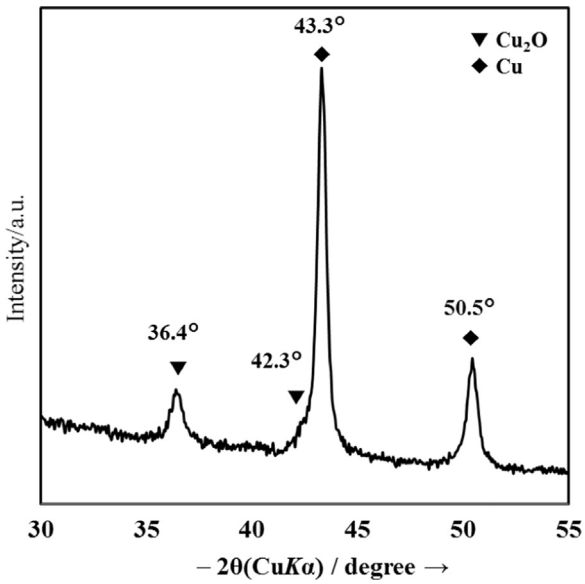

Fig. 1. XRD pattern of the resultant film with a thickness of 300 nm.

total Cu ion concentration was adjusted to 0.35 mmol g^{-1}. Next, Cu nano-powder (0.2 g) and five drops of 2-(2-butoxyethoxy) ethanol were added to the Cu precursor solution in an Ar-filled glove box, and the resulting mixture was ultrasonically stirred for 30 min

2.2. Dip coating and heat treatment procedures

The Si substrates with and without trenches were immersed in the Cu precursor solution under ultrasonic irradiation for 1 min, and then withdrawn slowly from the solution. The precursor films were preheated in a drying oven at 70 °C for 10 min and then heat-treated at 350 °C for 30 min under an Ar (99.99%, < 2 ppm O_2) flow of 1.5 L min^{-1} to fabricate thin films of copper in a tubular furnace with a quartz glass tube (40 mm diameter and 650 mm length). The ramping rate was set to 10 °C min^{-1} by adjusting the proportional, integral, and derivative values of the temperature controller. Before raising the temperature, the tubular furnace was purged with Ar gas. The dip coating and heat treatment steps were repeated to investigate the effect of layers.

2.3. Measurements

The crystal structure and phase of the heat-treated thin film adhered to the Si substrate was examined using an X-ray diffractometer with Cu Kα radiation at 45 kV and 100 mA. The XRD measurements were recorded using parallel beam optics with an incident angle of 0.3° in the 2θ range of 30–55°. The Si substrates coated with copper were cut into two pieces perpendicular to the trench. The cross-section images of the trench edge and film thickness of the heat-treated thin film were acquired using an FE-SEM. The topography measurements for the resulting thin films on the Si substrates with trenches were performed using an atomic force microscope. The central part within 2 μm wide coated trench was analyzed by Auger electron spectroscopy (AES) using an auger microprobe at a probe voltage of 10 kV and a beam diameter of 1 μmϕ. An Ar^+ ion beam at an acceleration voltage of 3 kV was used for 30 s to sputter etch the coating. The average relative concentrations of Cu, O, and C were determined by AES. Each AES spectrum at three different depths from the surface to 300 nm, of the thin film and trench, was measured after Ar^+ ion beam bombardment (3 kV) for 60 s. The electrical resistance of the resulting thin films on the Si substrate was measured at 25 °C using the four probe method.

3. Results and discussion

3.1. Crystal structure of the thin film on the Si substrate without a trench

The XRD pattern of the deposited thin film (300 nm) is shown in Fig. 1. The diffraction peaks at 2θ=43.3° and 50.5° are assigned to the (111) and (200) planes of copper (JCPDS card no. 04-0836) and the two additional peaks located at 36.4° and 42.3° can be assigned to the (111) and (200) planes of Cu_2O (JCPDS card no. 05-0667).

3.2. FE-SEM and AFM images of the single- and double-layer films on the Si substrates with trenches

The cross-section FE-SEM images of the single- and double-layer films on the Si substrates with trenches indicated that the embedded particles filled the trenches of (a) 1.0, (b) 0.5, and

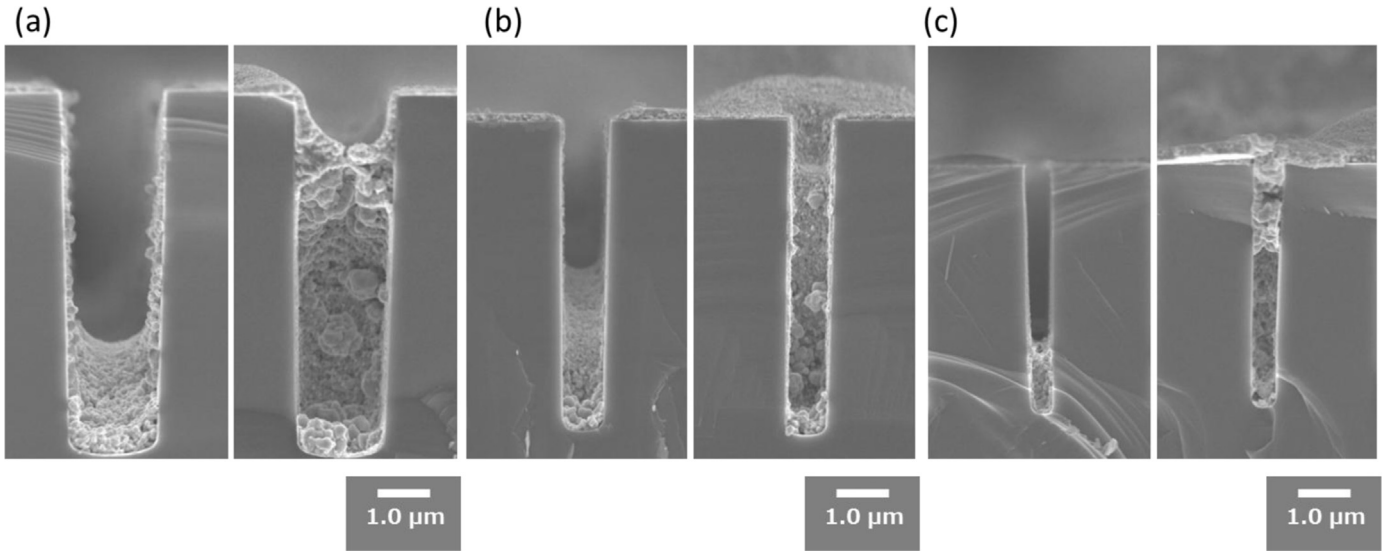

Fig. 2. Cross-section FE-SEM images of the single- and double-layer films on the Si substrate with trenches of (a) 1.0, (b) 0.5, and (c) 0.2 μm widths and 5 μm depth.