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Fabrication of single-crystal silicon nanowires based on surface wet adhesion

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ABSTRACT

In this paper, we present a top–down fabrication method of single-crystal silicon nanowires. The method employs the popular photolithography technique and etching-rate dependent on the crystal orientation of single-crystal silicon in KOH solution. Using surface wet adhesion and reduced silicon dioxide etching, nanoscale SiO_2 mask line patterns with width from 45 nm to 200 nm and length up to 120 μm are successfully patterned. The interspace between nanoscale SiO_2 mask lines is 750 nm, which is narrower than the 1.2 μm feature resolution of obtainable photolithography process. A mechanism for explaining the creation of nanoscale SiO_2 mask lines based on surface wet adhesion due to the capillary force is suggested and discussed. The single-crystal silicon nanowires have been successfully fabricated by transferring the nanoscale SiO_2 mask line patterns into the top silicon layer of SOI wafer by KOH anisotropic wet-chemical etching.

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1. Introduction

Silicon nanowires have shown many promising potential applications in nano-sensors, nanoresonators, and high-density integrated electronic and photonic circuits [1–3]. There are many efforts in the fabrication of silicon nanowires, which are classified into two approaches, bottom–up and top–down. In the bottom–up approach, a high level of composition and orientation control in semiconducting nanowires can be achieved by epitaxial growth [5–6]. However, assembling these nanowires into functional and highly integrated 2D or 3D heterogeneous architecture with high special and angular precision remains a major challenge, relying heavily on post-synthesis integration of various nanowires [7,8]. In the top–down approach, the crystal-single silicon nanowires can be fabricated by advanced lithography techniques such as electron beam lithography (EBL) or focused ion beam lithography and dry etching using fast atom beam (FAB) or deep reactive ion etching (D-RIE) [9–13]. The popular photolithography technique is normally used for producing features at microscale due to the limitations imposed by optical diffraction. Recently, there are few reports on innovative fabrication of silicon nanowires using the photolithography technique, deep reactive ion etching, and thermal oxidization [14–16]. These top–down processes are a high reproduction, mass production processes and relatively easy to form highly precise orientation structures compared to post-manipulation methods used in the bottom–up process.

In this paper, we report on a novel top–down fabrication method for creating single-crystal silicon nanowires based on surface wet adhesion and wet-chemical etching. The method employs the popular photolithography technique and etching-rate dependent on the crystal orientation of single-crystal silicon in KOH solution. In order to explain for the generation of nanoscale silicon dioxide mask lines, a surface wet adhesion mechanism due to the capillary force was suggested. Single-crystal silicon nanowires having width from 45 nm to 200 nm and length up to 120 μm have successfully transferred into the device layer of SOI wafer from nanoscale silicon dioxide mask lines using KOH anisotropic wet-chemical etching.

2. Design and fabrication

In order to investigate the proposed fabrication process, we design chromium mask three-line arrays with widths 1.2 μm, 1.3 μm, and 1.4 μm. Length of the chromium mask lines are 120 μm. Resolution between mask lines is 5 μm. Fig. 1(a) illustrates an array of the designed chromium mask line patterns.

The fabrication process of single-crystal silicon nanowires is schematically shown in Fig. 1(b)–(g). Here, we use the dependence of etching rate on the direction of crystal faces of single-crystal silicon material in KOH anisotropic wet etchant [17]. The fabrication

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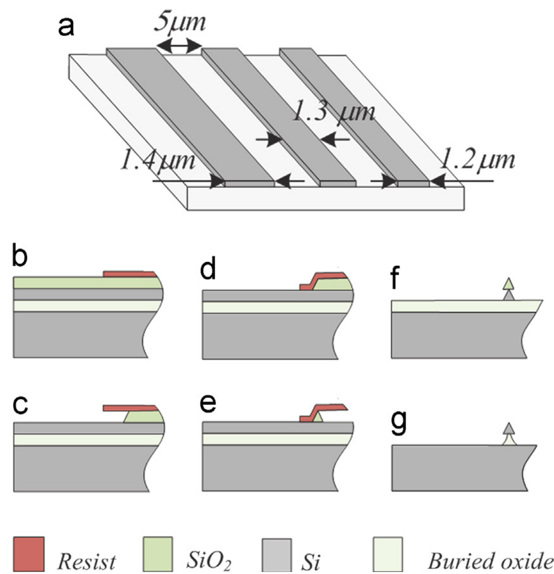

Fig. 1. Chromium mask three-line array is designed for investigating the fabrication process of single-crystal silicon nanowires (a). The fabrication process of single-crystal silicon nanowires is illustrated in Fig. 1(b)–(g).

process is started from SOI wafer having a device layer of 340 nm. The starting SOI wafer is oxidized for thinning the device layer to a desired thickness. In this work, the starting SOI wafer is oxidized in H_2O vapor at 1100 °C for 15 min to obtain a SiO_2 layer with the thickness of 140 nm. Thus, the silicon device layer remains to be 200 nm. We use the thermally formed SiO_2 layer as a mask layer for fabricating single-crystal silicon nanowires. Using the popular photolithography technique photoresist mask patterns are defined as shown in Fig. 1(b). Here, the 38 cp OFPA photoresist having low viscosity is selected to form thin photoresist layer for high resolution photolithography. The thickness of spin coating photoresist layer at the speed of 3000 rpm and the time of 30 s is measured to be 350 nm. The photoresist patterns are then post-baked in a heating oven at 120 °C for 10 min. After that wet undercut etching of SiO_2 is carried out in buffered hydrofluoric (BHF) solution (Fig. 1(c)). The thin photoresist mask layers is bended and then adhered to silicon surface using the capillary force as shown in Fig. 1(d) [18,19]. The wet undercut etching of SiO_2 is continued to form nanoscale SiO_2 mask line patterns as shown in Fig. 1(e). The wafer with nanoscale SiO_2 mask line patterns is then immerged in the 25% KOH solution at 80 °C. Under the anisotropic etching property of single-crystal silicon material, silicon nanowires are formed (Fig. 1(f)). The cross section of single-crystal silicon nanowires is triangular. Next, the buried oxide layer can be etched in BHF solution to form the structure shown in Fig. 1(g) or free standing single-crystal silicon nanowires.

3. Results and discussion

Fig. 2(a) is a scanning electronic microimage of an array of three SiO_2 mask lines. As seen in Fig. 2(a), the SiO_2 mask lines corresponding to the Cr mask line patterns with decreasing widths (1.4 μm, 1.3 μm, and 1.2 μm) have been sequentially separated, in which the SiO_2 mask line with the smallest width has been completely separated into the two lines. Fig. 2(b) shows a magnified scanning electronic microimage of the completely separated SiO_2 mask line. The SiO_2 mask lines are fairly uniform and smooth. The interspace between the SiO_2 mask lines are measured to be 750 nm, which is smaller than the resolution of used photolithography technique. The width of each separated SiO_2 mask line is 70 nm. The shape of nanoscale SiO_2 mask line are triangular. The shape of SiO_2 mask line is created by the isotropic etching of SiO_2 depending on BHF solution and etching time [20]. Fig. 2(c) shows another array of fabricated SiO_2 mask lines. The length of SiO_2 mask lines is measured to be 120 μm. In this case, the two SiO_2 mask lines with the smaller widths have completely separated into two lines. Fig. 2(d) shows a manified scanning electronic microimage of the two separated nanoscale SiO_2 mask lines. The widths of separated nanoscale SiO_2 mask lines are 50 nm and 200 nm, respectively.

The above experimental results show that the creation of nanoscale SiO_2 mask lines can be schematically illustrated in Fig. 3(a). States 1, 2, and 3 show the microscale SiO_2 mask line before separation, partially separated, and completely separated into two SiO_2 mask lines, respectively. In order to explain for the creation of the two nanoscale SiO_2 mask lines from one microscale SiO_2 mask line, a physical mechanism of this creation is proposed as follows. When the undercut etching process achieves a state as shown in Fig. 3(b), under the capillary force, the thin photoresist film is bent and then adheres to the silicon device layer with the removed SiO_2 mask layer (Fig. 3(c)). The silicon surface with completely removed SiO_2 layer is also considered to enhance the surface adhesion of resist film due to the H-passivated Si-surface. The BHF solution with the strong activity of HF acid will penetrate into microscale SiO_2 mask line through the two bended resist film edges and etch SiO_2 region at the center extending to the edges (Fig. 3(d) and (e)). The outside edges at both sides of the microscale SiO_2 mask line are protected by the photoresist layer temporarily adhered to the silicon device layer. The undercut etching process of SiO_2 layer at the line center is performed in following principle. The larger the contact area between the BHF solution and SiO_2 layer, the faster the etching rate (Fig. 3(f)). Therefore, the etching nucleation points from the line center are extended. The microscale SiO_2 mask line is then separated into two lines. If the etching process is continued, the two nanoscale SiO_2 mask lines are created. The inside edges of nanoscale SiO_2 mask lines become flat the same as those of the outside edges when the etching process of SiO_2 mask lines achieves a limitation state. In order to explain for separating microscale SiO_2 mask line with smaller width into two lines, reason may be because the photoresist mask line with smaller width become thinner compared to that with larger width after photolithography process. The diffusion of BHF solution through thinner photoresist layer is more effective than that through thicker photoresist layer, which leads to the etching process to the SiO_2 mask line with smaller width is faster.

Scanning electronic microimage of an array of the single-crystal silicon wires is successfully transferred from the array of SiO_2 mask lines. Fig. 4(b) and (c) are magnified images of partially separated microscale silicon wires at the middle and completely separated nanoscale silicon wires on the right in Fig. 4(a), respectively. From Fig. 4(c), interspaces between the nanowires at bottom and top are 250 nm and 600 nm, respectively. The widths of each nanowire at bottom and top are 45 nm and 340 nm, respectively. The etching time in the KOH solution was used to be 15 ± 3 s. The horizontal width of the sloped side is 145 nm, determined from Fig. 4(c). Using the anisotropic etching property of single-crystal silicon, the height of silicon device layer is estimated to be 205 nm, which is similar to the thickness of designed device layer. The width of single-crystal silicon nanowires can be reduced further by optimizing the thermal oxidization time to obtain the thinner silicon device layer or the wet-chemical etching process. In addition, in this work the SiO_2 mask line patterns have been transferred into the silicon device layer using KOH anisotropic wet-chemical etching. In order to obtain the width of single-crystal silicon nanowires the same as

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