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PII: S0257-8972(18)30256-1
DOI: doi:10.1016/j.surfcoat.2018.03.009
Reference: SCT 23189

To appear in: *Surface & Coatings Technology*

Received date: 4 December 2017
Revised date: 25 February 2018
Accepted date: 4 March 2018

Please cite this article as: Barnali Biswas, Yashodhan Purandare, Imran Khan, Papken Eh. Hovsepian , Effect of substrate bias voltage on defect generation and their influence on corrosion and tribological properties of HIPIMS deposited CrN/NbN coatings. The address for the corresponding author was captured as affiliation for all authors. Please check if appropriate. Sct(2017), doi:10.1016/j.surfcoat.2018.03.009

Effect of substrate bias voltage on defect generation and their influence on corrosion and tribological properties of HIPIMS deposited CrN/NbN coatings

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Abstract: Substrate bias voltage is one of the most influential deposition parameter for physical vapour deposition processes as it can directly control the adatom mobility during coating growth. It influences the hardness, roughness as well as the microstructure of the coatings. Thus, bias voltage could also affect the defect formation during the coating deposition. High Power Impulse Magnetron Sputtering (HIPIMS) has been proven useful in producing void free and arc droplet free dense coatings. However, such coatings can still suffer from some defects associated with external factors (independent of deposition technique), such as substrate irregularities and the flakes coming from the chamber components. In order to study the effects of bias voltage (U_b) on the defect formation during HIPIMS process, four sets of CrN/NbN coatings were deposited at U_b = - 40 V, - 65 V, - 100 V and - 150 V. Microscopic studies revealed that with the increase in bias voltage the coatings morphology was altered and the percentage of surface area covered by optically visible defects was increased from 3.13 % to 4.30 %. The defects on the coatings deposited at U_b = - 100 V and - 150 V led to preferential corrosive attack resulting in a sharp increase in corrosion current density during Potentiodynamic polarisation experiments. Room temperature pin-on-disc tribological tests exhibited the influence of defects on the wear behaviour; however, the coefficient of friction (μ) values were mainly influenced by the