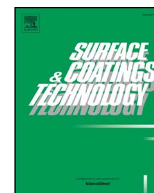
Surface & Coatings Technology xxx (xxxx) xxx–xxx

Contents lists available at ScienceDirect

Surface & Coatings Technology

journal homepage: www.elsevier.com/locate/surfcoat



Low temperature thin films for next-generation microelectronics (invited)

Jurriaan Schmitz

MESA + Institute for Nanotechnology, University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands

ARTICLE INFO

Keywords:
Integrated circuits
Coatings
Thin films
Deposition
Thermal effects
Thermal budget

ABSTRACT

In this article the current methodologies for low-temperature thin film deposition in microelectronics are reviewed. The paper discusses the high temperature processes in microchip manufacturing and describes the thermal budget fitting issue. The quest for low temperature deposition techniques is motivated in the perspective of contemporary trends in microchip technology such as 3D integration and the ending miniaturization. Reduced temperature depositions tend to deliver lower quality films. This is illustrated with the relation between deposition temperature and thin dielectric film quality (dielectric strength). Existing and emerging technologies for low-temperature thin film deposition are reviewed with an emphasis on their applicability in microelectronic fabrication.

1. Introduction

Microchip (integrated-circuit) fabrication has developed very rapidly since its inception in the late 1950s [1–3]. Propelled by the Digital Revolution, the global semiconductor industry today reaches annual sales close to 400 billion USD. Given the typical 15% R&D expenditure level of semiconductor companies in combination with their overall size, is it only to be expected that developments go fast and will continue to do so in the years to come.

While miniaturization long provided the heartbeat for innovation since the 1960s [4], the conventional lateral downsizing of components has today reached its limits [5]. Still, the demand for microchip innovation is all but diminishing. This leads to a broad search for improvements other than scaling [6]. The new paradigm for complementary metal-oxide-semiconductor (CMOS) and memory chips is called “equivalent scaling”: rather than physically miniaturizing the transistor, new materials and architectures are introduced to obtain the same performance benefits that lateral scaling used to bring [7]. This goes hand in hand with the renewed exploitation of the third dimension. Both for memories and digital logic, three-dimensional circuitry is rapidly being developed and brought to the market [8–10].

These developments pose several challenges to the involved materials scientists. First of all, the introduction of a new material into a microchip requires more than a successful thin film deposition. Good step coverage, in other words, conformal deposition is often a necessity, as high aspect ratio structures need to be coated; and the film needs to be patterned, requiring suitable etching processes. In addition, a thorough qualification must be carried out in order to safeguard the microchip's functioning and reliability. Novel materials may introduce new and unexpected reliability concerns that should be well understood and contained before mass production commences. In some cases, driven by commercial ambitions or changing legislation, market introductions appeared too early. For instance, the introduction of low-permittivity intermetal dielectrics and lead-free solder proved much more challenging than anticipated because of yield and reliability issues [11–13].

Another challenge can be described as “thermal budget fitting”. Each thin film has a typical deposition temperature and a certain thermal tolerance once deposited. The more films are stacked on top of each other, the more difficult it becomes to maintain the integrity of the already fabricated part, unless one gradually lowers the fabrication temperature. Indeed this is how microchips and many other planar-technology devices are made. Between the formation of the silicon substrate at 1414 °C and the final soldering of the chip onto a printed circuit board around 250 °C, the maximum temperature decreases as more and more layers are added to the substrate surface. This is illustrated in Fig. 1, and further discussed in Section 2.

The order of manufacturing steps, as well as the choice of materials, is often determined by thermal budget fitting considerations. One example is the replacement of aluminum by polysilicon for MOS transistor gates around 1970, enabling high temperature source/drain annealing after the formation of the gate [14]. Only in the most advanced CMOS generations metal gates were reintroduced, at the expense of complex replacement-gate procedures. Another example is the formation of (high-temperature) field isolation before the creation of transistors and diodes [14].

Several trends in microchip fabrication, most prominently the 3D integration mentioned above, demand the deposition of high-quality

E-mail address: j.schmitz@utwente.nl.

https://doi.org/10.1016/j.surfcoat.2017.11.013
Received 1 July 2017; Received in revised form 19 October 2017; Accepted 4 November 2017
0257-8972/ © 2017 The Author. Published by Elsevier B.V. This is an open access article under the CC BY-NC-ND license (http://creativecommons.org/licenses/BY-NC-ND/4.0/).

Please cite this article as: Schmitz, J., Surface & Coatings Technology (2017), http://dx.doi.org/10.1016/j.surfcoat.2017.11.013

ARTICLE IN PRESS

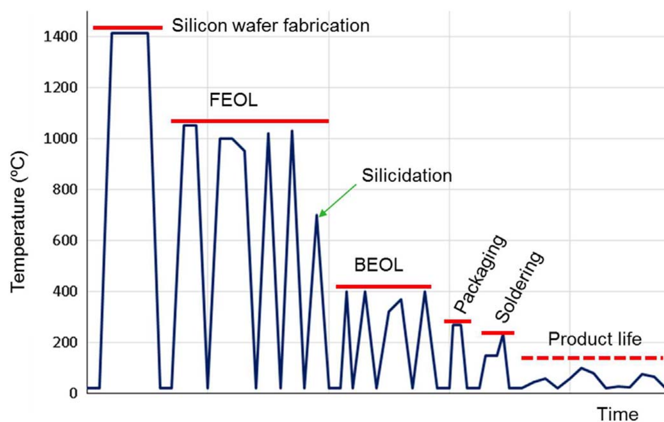


Fig. 1. Temperature excursions over time during the manufacturing process of a microchip and its functional life. First, wafers are manufactured at the silicon melting point; then follows field isolation and transistor fabrication (a stage known as front-end-of-line, or FEOL) at ~1000 °C. Silicidation takes place at a typical temperature of 500–700 °C depending on the reacting metal. The formation of the interconnections (back-end-of-line, BEOL) occurs at ~400 °C maximum. The chip is then packaged and soldered, after which the functional life commences, with uncertain thermal excursions.

conformal thin films at reduced temperatures. This article reviews the technological options for lower-temperature depositions in microelectronics. Here, conventional (thermal) chemical vapor deposition is taken as the starting point, as this is the traditional technology of choice in this application.

Section 2 of this article will further motivate the pursuit of low-temperature deposition techniques in the context of microfabrication. Section 3 treats six “cool” approaches for energy supply in order to control the formation of a good quality thin film. Section 4 concludes this article.

2. Deposition temperature: high or low?

Integrated circuits make use of thin films with the highest quality in terms of chemical composition, uniformity, defect density and electrical performance. Besides these properties, a thin film must adhere well and should not affect its surrounding layers by process induced damage or mechanical stress. Relatively expensive fabrication processes such as chemical vapor deposition, atomic layer deposition (ALD), deep-submicrometer lithography (including double patterning), plasma etching and chemical mechanical polishing are commonly applied in circuit fabrication. The economic value per unit mass of completed microchips exceeds that of pure gold and therefore, in comparison to most thin film applications, the priority is production yield before process cost.

High temperature process steps are common in integrated circuit manufacturing (cf. Fig. 1). These steps serve various purposes [15]: to activate impurities (dopants), repair lattice damage, deposit or densify materials; and to initiate reactions, mostly oxidation and silicidation. Impurity activation and lattice repair require temperatures of 900–1050 °C in silicon. Material depositions in integrated circuit processes typically take place at 600–850 °C (low-pressure chemical vapor deposition (CVD)), 300–400 °C (plasma-enhanced CVD) or close to room temperature (sputtering). A temperature between 700 and 1050 °C is used for oxidation of silicon. Silicidation is the reaction between a metal and silicon, carried out to form the electrically conducting interface between the semiconductor and the interconnect at a typical temperature up to 700 °C.

Microchip fabrication comprises several hundred process steps divided into several phases (depicted in Fig. 1). In every subsequent phase of this processing sequence, the maximum temperature goes down in order to maintain the chip's integrity. After the transistor fabrication phase, diffusion of impurities must be restricted. Once metallization is present on the chip, one should remain well below the metal melting temperature(s). After metallization and post-metal anneal, the hydrogen passivation of the silicon surface should remain intact. And after the final phase of soldering, the solder melting temperature should not be exceeded. The stack of layers in a microchip therefore goes “from hot to cold”, as depicted in Fig. 2. The use temperature range of integrated circuits spans from –40 °C to 150–175 °C. This also indicates a practical minimum temperature for the processing; there is no necessity to reduce the chip manufacturing temperatures below the maximum use temperature of 150–175 °C from a functional point of view.

The above considerations already indicate that lower temperature processes are preferred for process integration. Thermal budget fitting is easier if process steps are conducted at lower temperatures (and in shorter time spans). To fit all process steps of an envisaged microchip within a given budget of thermal excursions becomes more difficult when more layers (hence more process steps) are involved. This is the case in V-NAND FLASH memories where 32 to 64 stories of memory

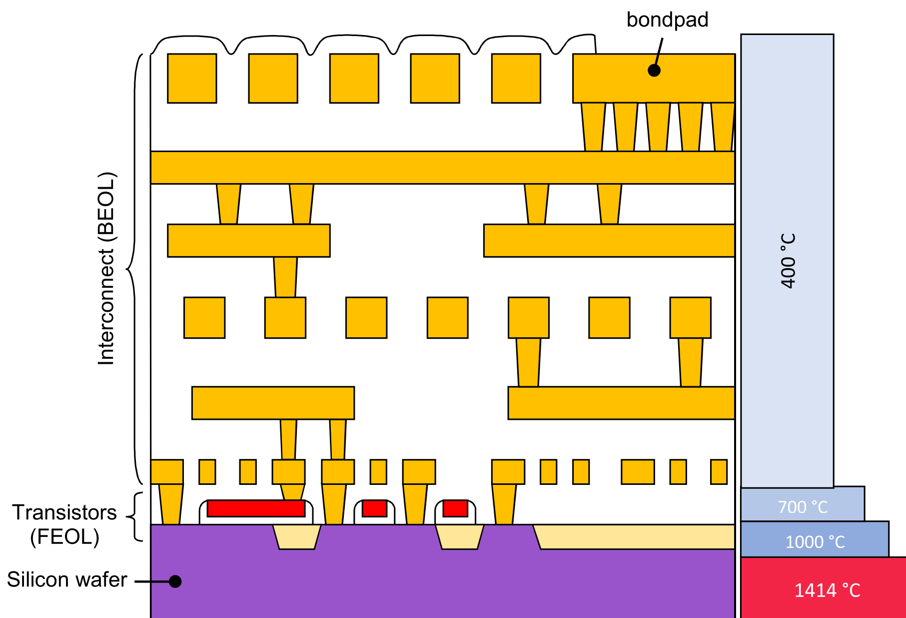


Fig. 2. Cross-section sketch of a silicon microchip, indicating the main production stages (as described in the caption of Fig. 1) and the related temperature limits.

Download English Version:

https://daneshyari.com/en/article/8023880

Download Persian Version:

https://daneshyari.com/article/8023880

Daneshyari.com