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In-line deposition of silicon-based films by hot-wire chemical vapor deposition

Lothar Schäfer [a,*], Tino Harig [a], Markus Höfer [a], Artur Laukart [a], Dietmar Borchert [b], Sinje Keipert-Colberg [b], Jutta Trube [c]

[a] Fraunhofer Institute for Surface Engineering and Thin Films IST, 38108 Braunschweig, Germany
[b] Fraunhofer Institute for Solar Energy Systems ISE, Laboratory- and Service Center LSC, Gelsenkirchen, Germany
[c] Leybold Optics GmbH, Alzenau, Germany

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ABSTRACT

Silicon-based films such as hydrogenated amorphous silicon (a-Si:H), nanocrystalline silicon (nc-Si:H), and hydrogenated amorphous silicon nitride (a-SiN_x:H) can be deposited by hot-wire chemical vapor deposition (HW-CVD). The HW-CVD technology differs from conventional plasma-enhanced (PE)-CVD in a number of technological aspects, such as soft activation, high growth rates, and low system costs. To evaluate the HW-CVD technology for thin film deposition in solar industry an in-line hot-wire CVD system was used to deposit a-Si:H films for passivation of crystalline silicon solar cells as well as for the fabrication of thin film silicon solar cells. The HW-CVD system consists of seven vacuum chambers including three hot-wire systems with maximum deposition areas of 500 mm by 600 mm for each hot-wire activation source. The deposition processes were investigated by applying design of experiment to identify the effects and interactions of the process parameters on the deposition characteristics and film properties. The process parameters investigated were silane flow, deposition pressure, substrate temperature, film thickness, as well as temperature, diameter and number of wires, respectively. Growth rates up to 2.5 nm/s were achieved for a-Si:H films. Intrinsic a-Si:H films for passivation of different crystalline solar cell types yielded carrier lifetimes of more than 1000 μs for film thickness values below 20 nm. For n-doped a-Si:H films prepared with PH_3 as dopant gas, electrical resistivity is in the range of 10^2 Ω cm. P-doped a-Si:H films prepared with B_2H_6 as dopant gas show electrical resistivity of about 10^5 Ω cm. Crystalline silicon heterojunction solar cells with intrinsic thin layer (HIT cells) exhibit energy conversion efficiencies of more than 17% when fabricated with intrinsic HW-CVD amorphous silicon films as passivation layers.

1. Introduction

The activation of silane containing gas phases by hot wires allows the deposition of high quality silicon-based thin films for a variety of applications [1–3]. The hot-wire activated chemical vapor deposition (HW-CVD) with pure silane gas results in amorphous (a-Si:H) [4] and nanocrystalline [5] silicon films. Dilution of silane with hydrogen yields nanocrystalline (nc-Si:H) silicon films, and addition of ammonia results in amorphous silicon nitride (a-SiN_x:H) films [6–8]. By using different precursor gases it is also possible to deposit thin film materials such as silicon carbide [9–13], SiCN [14] or germanium containing films like a-Si:Ge:H [15] and microcrystalline μc-$Ge_{1-x}C_x$ [16]. Despite the danger of wire oxidation even oxygen containing films can be produced by HW-CVD processes [17–20]. These different film materials are investigated for a wide range of applications [2] with a focus on solar cells and microelectronics. For these applications HW-CVD has a huge industrial potential due to the differences to conventional plasma-enhanced chemical vapor deposition (PECVD) methods. As there are no charged particles and electric fields involved, the deposition method is highly suitable for defect-free coatings and coatings on sensitive substrates [21]. High utilization of precursor gases yielding large deposition rates [22–24], and cost-effective deposition systems with high potential for scale-up [8,25] are additionally attractive for industrial applications of HW-CVD technology.

Amorphous silicon and silicon nitride films produced with HW-CVD processes have been investigated for the passivation of crystalline silicon solar cells [7,26–28]. Wang et al. [26] reported conversion efficiencies on p-type wafers of up to 19.3% for open circuit voltages (V_{oc}) of 678 mV, short-circuit current (J_{sc}) of 36.2 mA/cm^2 and fill factors (FF) of 78.6% on p-type float-zone silicon wafers with amorphous Si emitters deposited with HW-CVD processes. On p-type Czochralski Si wafers they achieved energy conversion efficiencies of 18.3% at V_{oc} of 670 mV, J_{sc} of 36.71 mA/cm^2 and FF of 76.5%.

Based on our HW-CVD results for thick intrinsic Si films and p- and n-doped amorphous Si for thin film solar cells [29] we investigated HW-CVD of thin intrinsic and doped amorphous silicon films for surface passivation and preparation of crystalline silicon solar heterojunction cells with intrinsic thin layer (HIT cells) [30,31]. The main focuses of this work were to understand how the passivation properties of intrinsic

* Corresponding author. Tel./fax: +49 531 2155 520.
E-mail address: lothar.schaefer@ist.fraunhofer.de (L. Schäfer).

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layers (i-layers) can be controlled by the deposition parameters and to process selected i-layers to complete HIT solar cells by using p- and n-doped a-Si:H films prepared by HW-CVD and PE-CVD, respectively. In order to elaborate the effects and interactions of several deposition parameters on the characteristics of the deposited coatings and the properties of the fabricated HIT cells, we used design of experiments (DoE) [32] for planning and analyzing experiments. Compared with the traditional way of experimentation where only one parameter (= factor) at a time is changed while all other parameters are kept constant, in DoE all factors to be studied are changed simultaneously on defined levels. The ensemble of all combinations of factor levels where experiments (= deposition runs) are performed is called experimental design and is chosen by algebraic and group theoretic arguments in order to get maximum information at minimum effort. The results of the experiments are called responses to the factor combinations. One main advantage of DoE is that analysis yields a mathematical model for each measured response which is valid for the complete volume of the multi-dimensional factor space enclosed by the design points.

The novelty of this paper lies in the production of intrinsic silicon layers by using an inline hot wire CVD process allowing the continuous deposition of silicon wafers with constant properties such as carrier lifetime over a width of more than 350 mm perpendicular to the substrate movement. Applying DoE interdependencies between seven deposition parameters could be investigated simultaneously resulting in a more general understanding of the deposition process of i-layers with high carrier lifetimes than one factor at a time approaches. These results have been used to produce HIT cells with relatively high performance. Despite the performance at this stage of the investigations not as high as the Sanyo HIT cells, which have been optimized for decades with PECVD processes and those reported on laboratory scale for HWCVD [26] the results of these investigations open a new route for highly cost-effective production of HIT solar cells with acceptable performance.

2. Experimental details

For the hot-wire chemical vapor deposition of the amorphous silicon-based coatings a seven-chamber inline coating system consisting of two load lock chambers with heaters, three HW-CVD chambers, and two intermediate chambers equipped with a heater system and a plasma etcher, respectively, was used. The deposition chambers are equipped with planar vertical multi-wire arrays each with parallel tungsten wires offering an activation area of 600 mm by 500 mm resulting in deposition areas of 400 mm × 400 mm with film thickness deviations of less than ±5% and essentially constant carrier lifetime values. Wire arrangements with two different wire diameters (0.25 and 0.5 mm) and two different wire-to-wire distances realized by using arrangements with 10 and 17 wires, respectively, have been investigated.

The deposition rates and the passivation properties of intrinsic a-Si:H films prepared by HW-CVD were studied by applying high resolution factorial designs. In total, the influences of the seven factors shown in Table 1 were investigated. Basically, each factor was varied only at two levels, a lower one (−1) and a larger one (+1). Changes in the factors F (wire diameter) and G (number of wires) were associated with a change of the filament setup. By keeping the activation areas approximately constant four filament setups were used combining 10 and 17 tungsten wires with diameters of 0.25 and 0.50 mm, respectively. All depositions with the same filament setup were carried out in succession. In order to control the film thickness (factor D) for each filament setup at first the influences of the factors silane flow (A), pressure (B), wire temperature (C), and starting temperature (E) on the deposition rates had to be measured which was done in separate experimental designs for film thicknesses (factor D) of about 150 and 600 nm, respectively. With the resulting control of the deposition rates over the complete factor space, all a-Si:H depositions for the given experimental design were carried out in fully randomized order. Additionally, for each filament setup five so called center points – i.e. experiments with the factors A–E set to the averages of the corresponding −1 and +1 levels – were carried out to check reproducibility and the existence of non-linear effects. In total, for each filament setup 16 intrinsic a-Si:H films with different combinations of the factors A–E plus 5 center points were prepared with the same wires enabling the estimation of main effects and two-factor interactions. The experimental designs for all four filament setups were constructed in a way that the combination of all sub-designs provides a total DoE for seven factors with resolution VII enabling even the evaluation of three-factor interactions. In each deposition run four Si wafers were deposited: two textured n-type wafers with resistivities of 1 and 3 Ω cm, respectively, and two bright etched wafers with 1 Ω cm of type n and p used as references. For selected factor settings it has been proven that the positions of all four wafers were equivalent to each other. Simultaneous deposition of four wafers of the same type yields effectively identical carrier lifetimes.

Table 1
Factors and factor levels used in the factorial design of experiments (DoE) for studying the deposition rates and the passivation properties of intrinsic a-Si:H layers. Basically, each factor is varied at lower (−1) and higher (+1) levels. Additionally, for each filament setup five local center points with factors A–E at the average value of the −1 and +1 levels were prepared for checking reproducibility and the importance of non-linear effects.

				−1 Level	+1 Level
1	A	SiH_4 flow	sccm	90	150
2	B	Pressure	Pa	1	2
3	C	Wire temperature T_{wire}	°C	1900	2100
4	D	Film thickness	nm	7	20
5	E	Initial substrate temperature T_{start}	°C	120	200
6	F	Wire diameter	mm	0.25	0.50
7	G	Wire number	mm	10	17

During the pump-down and degasing step in the lock chamber the wafers were preheated to about 100 °C. Then the substrates were transferred to a separate chamber with a second heater system set to a fixed surface temperature of 390 °C. After residence times of 2 and 9 min, respectively, the two levels of the initial wafer temperature T_{start} = 120 °C and 200 °C (cf. Table 1, factor E) were achieved. Thereafter the deposition was carried out by moving the substrate carrier through the close-by deposition chamber where the deposition conditions (factors A, B, and C) for the given setup have been already stabilized during the pump-down and heating procedures. The speed of the substrate carrier and the residence time of the carrier in the deposition chamber were chosen according to the desired film thickness and the growth rate for the given set of deposition parameters. Due to the large range of investigated factor settings two different types of deposition procedures have to be used: The 7 nm films and the 20 nm films with high deposition rates were prepared by moving the substrate carrier with constant velocities of 40–150 mm/s through the deposition chamber (dynamic deposition). For about one third of the 20 nm films the required carrier speeds for dynamic deposition were too slow to keep the initial substrate temperature T_{start} close to the level defined in the heating system since at such low carrier speeds during transport cooling-down happens when facing colder parts of the reactor system. In these cases, after moving the substrate carrier to the center of the deposition chamber with 150 mm/s, movement was interrupted for a defined holding time, and thereafter the carrier system was moved out of the deposition chamber again with 150 mm/s (interrupted deposition). For the deposition of the doped films with thicknesses of 20 nm interrupted/dynamic deposition procedures were used, as well.

The temperatures of the wires T_{wire} (factor C) were controlled by an optical ratio pyrometer. After the deposition of the i-layer the carrier was locked-out to air. The wafers were turned around and the back sides were deposited with the same set of parameters shortly after the first deposition without additional HF-dip. After all depositions for