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Grain-scale adhesion strength mapping of copper wiring structures in integrated circuits

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ABSTRACT

The adhesion strength distribution at the interface between damascene copper lines and the cap layers covering the lines was explored. A novel system composed of a dual-beam SEM/FIB equipped with a nanoindenter and an EBSD camera enabled successful evaluation with a resolution of the order of 300 nm, which is the scale of crystal grains. The adhesion strength was found to scatter in a range spanning roughly half to double the average value. Although no clear correlation was observed with the geometry of the copper line, the impact of the copper grain structure beneath the specimens was rather distinct, where the adhesion strength of specimens with grain boundary junctions observed on their footprints was significantly lower than that of specimens without junctions. This result suggests that the microscopic structure of deposited materials may strongly influence the strength of adhesion to neighboring layers. Therefore, the evaluation of local adhesion is important from an engineering point of view as a means for avoiding unexpected fractures at possible weak points and assessing the mechanical reliability of the layered systems.

1. Introduction

The adhesion of deposited materials may not be homogeneous over the entire substrate surface. Especially in the case of patterned thin film structures, the processing parameters and the material structure may display local variations leading to an inhomogeneous distribution of the adhesion strength. Such fluctuations in strength can cause unexpected local damage due to stress arising during the fabrication and operation of microscale devices. For example, three-dimensional stacked copper interconnect structures in large-scale integrated circuits (LSIs) frequently suffer from unexpected fractures during fabrication, especially at the interfaces between layers [1–3]. In spite of the intensive effort to devise methods for preventing such damage, fracture remains a threat that increases the risk and thus the cost of development. The most likely reason for this is that the design essentially relies on data about macroscopic average strength.

The interface adhesion strength in multilayered materials has been commonly obtained from macroscale specimens with blanket films of composing materials by applying conventional techniques such as scratch tests [4] and indentation tests [5–8]. However, these tests induce complex fractures with cracks not only along the interface but also inside the layers, and thus may not be suitable for exclusive evaluation of the local adhesion strength in sub-micrometer scale structures such as LSIs. In the LSI industry, the most commonly applied technique for adhesion measurement is the four-point bending test [9–11], which evaluates the fracture resistance of interface cracks, however, it uses specimens with dimensions in the order of millimeters. Therefore, such tests are unable to provide any information about possible microscopic weak points from which cracks may extend.

A recent study found that the fracture energy of the interface between a copper line and a barrier layer is affected by both the composition of the barrier and the purity of electroplated copper, and that impurities are segregated at grain boundaries and their triple junctions [12]. These results suggest not only that the fabrication process affects the adhesion strength, but also that grain boundaries in copper lines are responsive for inducing fluctuations in the local adhesion strength in interconnect structures. Furthermore, stress- and electromigration are already known to be strongly dependent on grain boundary structures and triple junctions of grain boundaries [5,13,14]. For this reason, the strength of adhesion to neighboring layers is also expected to be

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highly sensitive to the presence of grain boundaries. Therefore, a testing method with a range of resolutions corresponding to the dimensions of the examined material structures, such as crystal grains, is necessary for evaluating the local distribution of interface adhesion and mapping the strength of microstructural components.

As a solution to the problem of evaluating local strength distribution, the authors developed a micrometer-scale technique allowing the evaluation of the local strength of interfaces in terms of adhesion energy [15–18], where microscale specimens were fabricated directly from stacked thin film structures and delaminated at the interface of interest. In a report where this technique was applied to damascene interconnect structures in LSIs, local fluctuations in the adhesion strength at the interface between copper lines and a SiN cap layer were already suggested for specimens with a square base of 10×10 μm [19].

In this paper, a similar interconnect structure was evaluated with submicron-scale resolution in a novel system developed recently for performing in-situ fracture tests while conducting observations with a scanning electron microscope (SEM) [20], where a dual-beam system consisting of a SEM for observation and a focused ion beam (FIB) for specimen fabrication is further equipped with a nanoindenter for applying mechanical load to specimens and an electron backscattering diffraction (EBSD) camera for crystal grain analysis. Taking advantage of the sufficiently high resolution of the SEM/FIB system, specimens with sub-micrometer dimensions were fabricated and tested to evaluate the local distribution of adhesion strength, that is, to map possible trends in adhesion strength with respect to the geometric position in interconnect structures. In addition, the crystallographic orientation of copper grains at the fracture sites was also examined in view of possible correlation between the distribution of strength and grain structure. By gathering this information, local weak points in LSI metallization systems were explored from the perspective of minimizing the risk of unexpected fractures, which is the goal of this study.

2. Experimental

2.1. Specimen fabrication

A schematic illustration of the interconnect structure tested in this study is shown in Fig. 1(a). The weakest interface in this structure is between the upper surface of the copper line and the SiN cap layer, and the adhesion strength at that interface was examined. Two types of specimens (denoted as A and B) were fabricated for the fracture test by using an FIB to cut the upper SiO_2 layer into blocks with square bases and to remove the surrounding parts to expose the bare surface of the copper line around the specimens as shown in Fig. 1(b). Type A specimens, designed with in-plane dimensions of 500×500 nm, were lined across a 20-μm-wide Cu line in order to obtain the local distribution of adhesion strength in transverse direction. Furthermore, type B specimens with in-plane dimensions of 300×300 nm were lined along the center line of a 600-nm-wide copper line to examine the distribution in longitudinal direction. After trimming the SiO_2 layer with the FIB, amorphous carbon was vacuum-deposited onto the structure to a thickness of less than 10 nm in order to prevent electron charging during the fracture test under SEM observation. The average grain size was 1.1 μm for the 20-μm-wide line and 450 nm for the 600-nm-wide line.

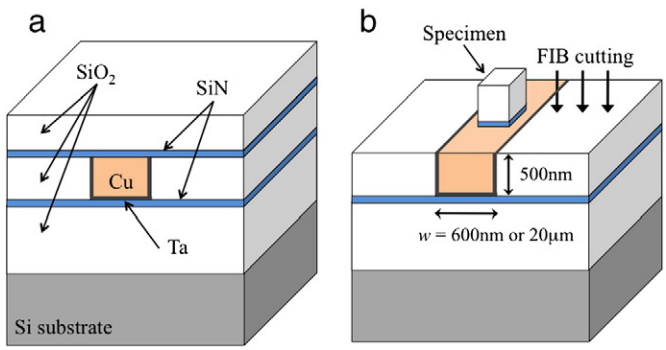

Fig. 1. (a) Interconnect structure and (b) a fabricated specimen. Specimens with a base of 500×500 nm (type A) were fabricated on a 20-μm-wide copper line, and specimens with a base of 300×300 nm (type B) were fabricated on a 600-nm-wide copper line.

2.2. Fracture test using submicrometer-scale specimens

As a means for evaluating the local interface strength with submicrometer resolution, a novel system allowing for in-situ fracture tests under SEM observation was recently developed by combining a nanoindenter (PI-85, Hysitron Inc.) with an FIB–SEM dual-beam microscope (JIB4600F, JEOL Ltd.) [20]. The setup in the microscope chamber is shown in Fig. 2(a). The same experimental procedure was applied for the fracture test of both types of specimens. Fig. 2(b) shows a scanning electron micrograph of the area around the stylus tip in the fracture test of a type B specimen, which was designed as a square-based block but appeared with rounded corners due to the resolution provided by the FIB. A diamond stylus with a tip radius of 0.1 μm was used to apply lateral load with the nanoindenter to the specimen approximately 100 nm above the Cu/SiN interface in order to initiate a crack which extends stably at the interface. The details of the loading points were observed for each individual specimen in the experiment, and the results were reflected in the simulation of interface crack extension explained in the following section. The stylus was driven parallel to the surface of the Si substrate at a speed of 10 nm/s, and the load and displacement were measured at a sampling rate of 200 Hz. During the test, the specimen was pushed off at a certain amount of load and the load suddenly dropped to zero. Panels (a) and (b) in Fig. 3 show scanning electron micrographs of a type B specimen before and after the experiment, respectively, and Fig. 4 shows a typical load–displacement curve. The maximum load measured during the fracture test was employed for the evaluation of the adhesion strength on the basis of the numerical simulation presented in the following section.

3. Numerical simulation for the evaluation of adhesion strength

The crack extension behavior at a Cu/SiN interface was simulated by elastic finite element analysis under the assumption of linear elastic deformation. Fig. 5 shows the finite element model prepared for a type B specimen. The material properties used in the finite element analysis are summarized in Table 1, where the Ta layer was ignored as it was considerably thinner than the other layers. Young's modulus of copper was obtained by a nanoindentation technique applied to the same test structure. The residual stress in the SiO_2 layer was measured on the basis of the wafer curvature, and the obtained value of −130 MPa was employed in the finite element model. The point where the stylus touched each specimen, that is, the location where load was applied, was identified by scanning electron microscopy and reflected in the model of the specimen.

When external load was applied, the amount of energy released per unit area of interface crack extension (energy release rate) was estimated at all nodes along the crack front by using a virtual crack extension method where the applied external load was increased until the maximum of the energy release rate for the nodes reached a constant critical value defined in advance. At that stage, the node where the energy release rate was in balance with the critical value was divided into two nodes at both sides of the interface in order to simulate crack extension. By repeating this procedure, the load required to further extend the interface crack was obtained as a function of the crack extension area. An example of the simulated crack extension behavior is shown in Fig. 6, where the abscissa indicating the area of crack extension is normalized with respect to the total area of the specimen footprint. Consequently, the specimen was