Solar Energy Materials & Solar Cells 92 (2008) 1352–1357

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Fabrication of nanoporous antireflection surfaces on silicon

Mao-Jung Huang [a], Chii-Rong Yang [b,*], Yuang-Cherng Chiou [a], Rong-Tsong Lee [a]

[a] Department of Mechanical and Electro-Mechanical Engineering, National Sun Yat-Sen University, Kaohsiung 804, Taiwan
[b] Department of Mechatronic Technology, National Taiwan Normal University, 162, Sec. 1, Ho-Ping E. Road, Taipei 106, Taiwan

ARTICLE INFO

Article history:
Received 28 December 2007
Accepted 19 May 2008
Available online 1 July 2008

Keywords:
SANSL
PAECE
Nanopore array
Antireflection structure

ABSTRACT

After the surface of a silicon wafer has been texturized, the reflectance of the wafer surface can be reduced to increase the power generation efficiency of a silicon-based solar cell. This study presents the integration of self-assembled nanosphere lithography (SANSL) and photo-assisted electrochemical etching (PAECE) to fabricate a nanostructure array with a high aspect ratio on the surface of silicon wafer, to reduce its reflectance. The experimental results show that the etching depth of the fabricated nanopore array structure is about 6.2 μm and its diameter is about 90 nm, such that the aspect ratio of the pore can reach about 68:1. The weighted mean reflectance of a blank silicon wafer is 40.2% in the wavelength range of 280–890 nm. Five-minute PAECE without SANSL reduces the weighted mean reflectance to 5.16%. Five-minute PAECE with SANSL reduces the weighted mean reflectance to 1.73%. Further coating of a 200 Å thick silicon nitride layer on the surface of a nanostructure array reduces the weighted mean reflectance even to 0.878%. The novel fabrication technology proposed in this study has the advantage of being low cost, and the fabricated nanostructure array can be employed as an antireflection structure in single crystalline silicon solar cells.

1. Introduction

In recent years, many studies have been performed on the surface texture of silicon wafer [1–5]. The purpose is to produce a micro/nanostructure on the surface of silicon wafer, to reduce the reflectance of the silicon wafer, and increase the power generation efficiency of the silicon-based solar cell Because when the surface of the silicon wafer has a subwavelength structure (SWS) that is smaller than the wavelength of light and the structure has a periodic arrangement, a strong antireflection effect can be produced [5]. Usually, the random pyramid antireflection structure is currently used for the texturization of the silicon solar cell [6]. The random pyramids on the silicon surface are produced in KOH or NaOH etchant after etching for about 40 min at an etching temperature of over 70 °C. Although such an alkaline etching technique is simple and low cost, it has drawbacks of being time-consuming, requires heating and yields poor uniformity The etching solution must be mechanically agitated for better uniformity of the textured structure on silicon surface [7] Besides, the presence of alkali metal ions in KOH or NaOH etchant, incompatible with IC processing, may be detrimental to the fabrication of a silicon-based solar cell.

Traditionally, advanced lithography methods such as electron-beam (E-beam) [8] or focus ion-beam (FIB) [9,10] and deep ultraviolet lithography (DUV) [11,12] are adopted to define periodic nanoscale patterns. Afterwards, inductively coupled plasma reactive ion etching (ICP–RIE) or electron cyclotron resonance (ECR) plasma etching can be used to form silicon nanopore or nanopillar array structures with high aspect ratios [11–14]. Although such methods can be used to define the nanoscale pattern precisely, they are not suited to fabricate a large-area structure, because the process is time-consuming, and the cost of equipment or process is very high. Moreover, the nanoscale array pattern can be also defined on the surface of the silicon wafer by the self-assembly of a polystyrene nanosphere [15–17], and the shape and size of the pattern can be determined effectively by appropriately selecting the size of the sphere and controlling the layer number of nanosphere. This fabrication method is also called self-assembled nanosphere lithography (SANSL). Similarly, the expensive ICP-RIE etching procedure must be employed to form a silicon array structure with a high aspect ratio [18].

This study combines the SANSL process and photo-assisted electrochemical etching (PAECE) to fabricate a nanostructure array with a high aspect ratio on the surface of a silicon wafer, to fabricate the antireflection structure of a silicon-based solar cell. In fact, PAECE is a well-known etching approach [19–25]. It has the advantage of being low cost, and the aspect ratio of etched nanopores can be as high as 250:1 [26]. Some studies have applied

* Corresponding author. Tel.: +886 2 23583221x14; fax: +886 2 23583074.
E-mail address: ycr@ntnu.edu.tw (C.-R. Yang).

0927-0248/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.solmat.2008.05.014

PAECE technique to produce photonic crystals [27–29]. PAECE technique can also overcome the drawback of reactive ion etching (RIE) lag [30]. RIE lag is a frequently seen defect during a plasma etching process, especially found in etching high-aspect-ratio trenches into silicon. In general, smaller trench openings are etched slower than those that are wider, significantly affecting etching uniformity of the feature geometrical shape.

This study combines SANSL and PAECE techniques to fabricate a periodic nanostructure array on the surface of a silicon wafer as the antireflective structure of a silicon-based solar cell. Compared to the fabrication method of the currently used random pyramids, our approach can form the periodic nanostructure array as antireflection surface under the conditions of short etching time, room temperature, and without the presence of alkali metal ions in hydrofluoric acid (HF). Except evaluating the etching characteristics of PAECE, the effects of experimental parameters on the reflectance are also discussed under the conditions of whether SANSL is conducted and whether a silicon nitride layer is coated on the surface of nanostructure array.

2. Experimental design

Fig. 1 shows the flow chart for the fabrication of a periodically arranged nanopore array. The major processes are SANSL and PAECE, and the experimental steps are detailed as follows.

This study uses a 4-in (100 mm) N-type silicon wafer. The resistance of the silicon wafer is $0.01-0.018\,\Omega$/cm, and its thickness is 525 μm. A 200 nm thick layer of silicon nitride is initially deposited on the wafer surface by low pressure chemical vapor deposition (LPCVD), and is used as an etching mask in PAECE. The wafer is cut to 18×18 mm to fit the etching tank. A 2.5% (w/v) suspension of polystyrene nanosphere (200 nm diameter) (Polysciences, Inc.) is mixed with methanol and Triton X-100 (surfactant) in a volume ratio of 800:400:1.

Before nanospheres are spin-coated, the sample is cleaned in the ultrasonic vibrator using piranha solution ($H_2SO_4 : H_2O_2 = 3 : 1$ by volume), acetone and methanol for 1 h, 30 min and 30 min, respectively, at a vibrating power of 100 W. It is rinsed in deionized (DI) water for 5 min to eliminate cross contamination between any two aforementioned cleaning processes. Finally, the sample is maintained in methanol. A 1–1.2 ml volume of the suspension of polystyrene nanospheres is dropped on the sample. Spin coating is performed at 1300 rpm to arrange the nanospheres uniformly on the sample. The coated sample is placed on the hot plate, and baked at 40 °C for 5 min to remove the solvent. RIE is used to etch the exposed silicon nitride among the nanospheres in 10 sccm of CF_4 at 60 m Torr and 180 W for 12 min, to generate the etching window of PAECE. Finally, the sample is placed in dichloromethane and acetone to remove polystyrene nanospheres. After these steps have been completed, the pattern of nanospheres can be transferred into a silicon nitride layer, and then the PAECE process implemented.

The PAECE process was performed according to the experimental scheme shown in Fig. 2. The potentiostat (EG&G Model 263A) was adopted to apply a positive bias to the sample, and the distance between the platinum cathode and the anodic sample was 4 cm. A 340 W xenon lamp was applied to radiate the back of sample, and the distance between the radiating source and the sample was 7 cm. The conductive layer of the anode electrode was composed of chromium film (5 nm) and copper film (200 nm), which were deposited at the back of sample, such that the etching bias voltage was distributed uniformly on the sample. The HF concentration of the electrolyte used herein was 2.5 wt% (DI water: ethanol: HF (50 wt%), 14:5:1 by volume). The area of the sample exposed to the electrolyte was 1.13 cm^2. An etching

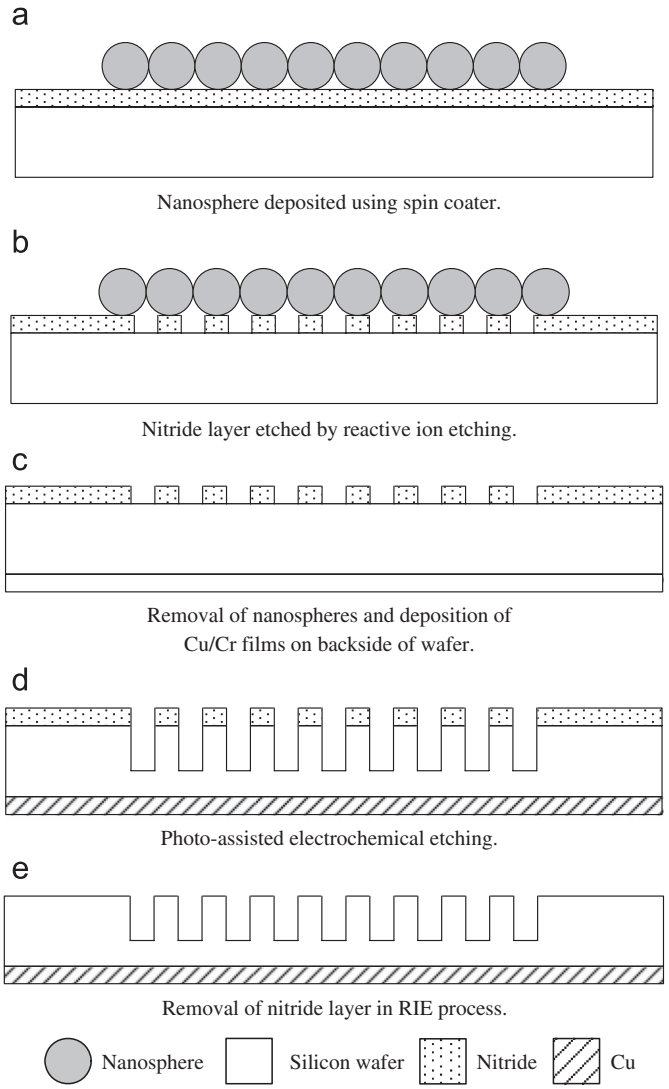

Fig. 1. Process flow for fabricating periodic nanopore array structure.

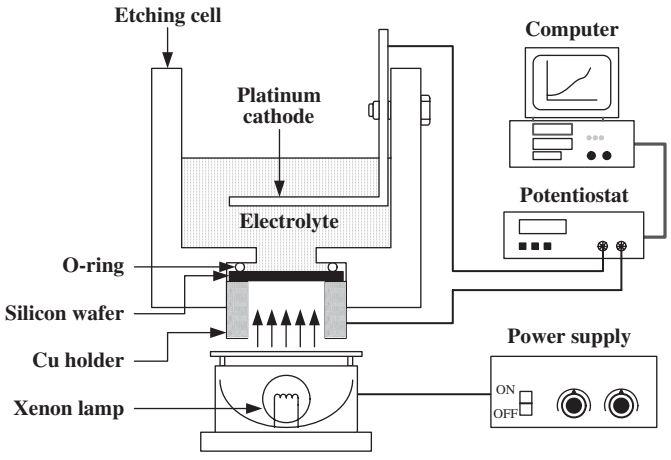

Fig. 2. Schematic diagram of PAECE setup.

voltage of 1 V was used, and the etching time was set 2.5, 5, 7.5, 10 and 12.5 min. The etching temperature was 22 ± 1°C, and no agitation was used in the experiment. After the PAECE process had been completed, the periodic array of nanopores was formed, and the RIE was then used to remove the silicon nitride layer from the