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Effect of interfacial layer on device performance of metal oxide thin-film transistor with a multilayer high-k gate stack

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ABSTRACT

The amorphous indium gallium zinc oxide thin-film transistors (TFTs) with a multilayer high-k gate stack are investigated in this research. In order to achieve a high quality gate insulator for plastic flexible display application, the multilayer high-k gate stacks ($SiO_2/TiO_2/HfO_2$) are deposited by a low-temperature physical vapor deposition (PVD) process. On the other hands, an interfacial layer between the high-k stack and metal oxide channel is important for the device performance. The effects of interfacial layer material (SiO_2 or Ga_2O_3) are also discussed in this report. The devices with SiO_2 interfacial layer show a high on/off current ratio of ~7×10^7 for its low gate leakage current, a small sub-threshold swing of 0.093 V/decade and a high field-effect mobility of ~37.8 cm^2/Vs for its good interface condition and low interface defeats. This research shows that the interface engineering of multilayer PVD gate stacks is necessary for oxide TFT fabrication.

1. Introduction

Recently, transparent amorphous oxide semiconductor (TAOS) has attracted many attentions for its excellent electrical performance and transparent characteristics [1]. Among many TAOS materials [2–5], the amorphous indium gallium zinc oxide (a-IGZO) is the most potential candidate serving as semiconductor layer in thin film transistor (TFT) due to its low off-current (I_{OFF}) originated from its large energy band gap and high mobility of overlapped s-orbitals. Moreover, high dielectric constant (high-k) gate insulator was widely investigated in a-IGZO TFTs to achieve low operating voltage owing to their outstanding capability of gate control [6,7]. Besides, some multilayer high-k structure, like, $SiO_2/Ta_2O_5/SiO_2$ [8], $Al_2O_3/HfO_2/Al_2O_3$ [9], $SiO_2/HfO_2/SiO_2$ [10], are proposed to further improve the field effect mobility and adjust the negative threshold voltage. However, it is difficult to achieve large on/off current ratio and higher mobility simultaneously. Although some works exhibit many advantages such as low gate-leakage current and higher stability, there are still several drawbacks for high-k gate insulators such as large surface roughness and low band offset barrier, which may restrict the carrier mobility and standby power consumption [11,12]. Therefore, the interfacial layer engineering is necessary for the TFT device performance, while the interfacial layer material and effect are worthy of further discussion.

In the present work, a multilayer high-k gate insulator $HfO_2/TiO_2/SiO_2$ structure (HTS) is proposed to increase the effective dielectric constant and reduce the device leakage current. In addition, two types of high quality interfacial layer materials, SiO_2 and Ga_2O_3, are selected for comparison, in order to either improve the surface morphology between the channel layer and multilayer gate insulator after the inevitable thermal process or enlarge the energy band offset between the HfO_2 and channel material without introducing more interface defeat states. The mechanisms for enhancement of electrical characteristics are also well discussed in detail by the physical analysis and operation energy band model of a-IGZO TFT.

2. Experiment

TFT devices with bottom gate staggered structure were fabricated on a doped n-type Si wafer with 100-nm thick thermal buffer oxide layer grown on top. The gate electrodes were then formed and patterned by sputtering 60-nm thick TaN thin film through a shadow mask. Then, a multilayer gate dielectric stack of 3-nm SiO_2, 30-nm TiO_2 and 40-nm HfO_2 was deposited as gate insulator (GI) layer by electron gun evaporation. Afterward, two types of interfacial layer was deposited in the in-situ chamber, using with 1-nm thick SiO_2 interfacial layer or 1-nm thick Ga_2O_3 interfacial layer which named SHTS GI sample and GHTS GI sample, respectively. Simultaneously, the multilayer high-k TFT device without interfacial layer named HTS GI sample is used as

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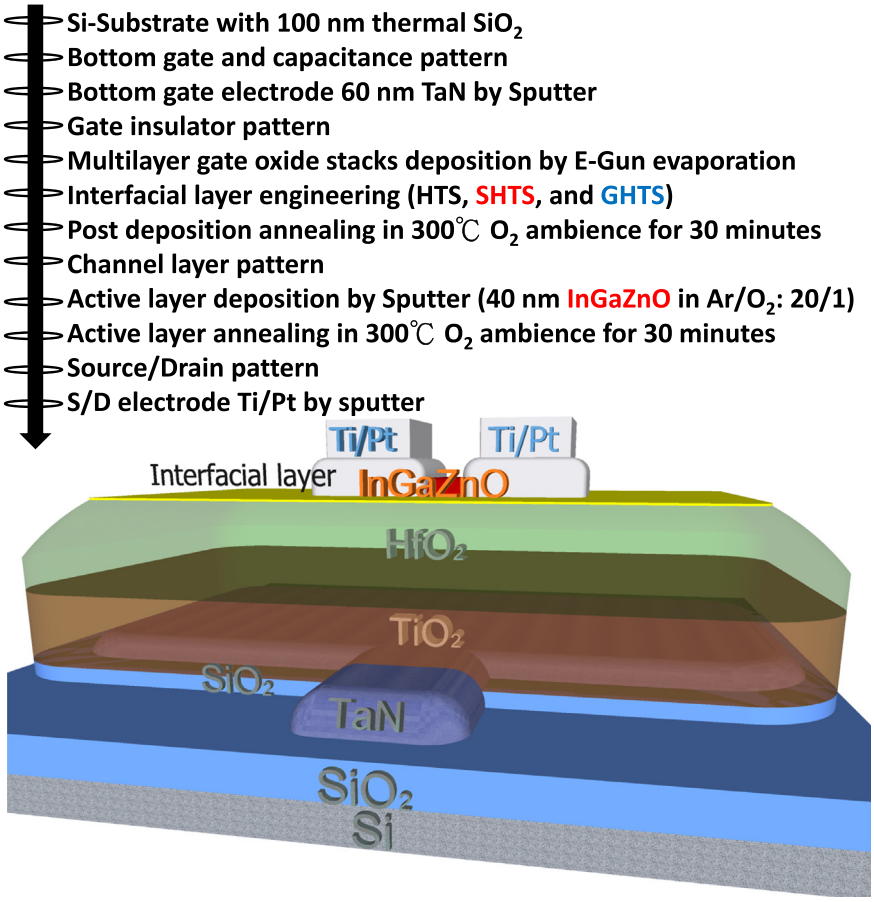

Fig. 1. 3D structure view and schematic process flow in this work.

the control one. After the multilayer GI layer deposition, a post deposition annealing was performed at 300 °C in oxygen ambient for 30 min by a thermal furnace, in order to improve the quality of dielectrics film and fix the bulk defeats in the multilayer GI. After gate region formation, a 40-nm thick a-IGZO thin film was deposited as the channel layer by RF magnetron sputtering process using a target with the atomic ratio of In:Ga:Zn:O = 1:1:1:4 at room temperature. During the deposition, the flow rate of O_2 and Ar was set at 1 and 20 sccm, respectively. The total gas pressure in the sputter chamber was controlled to be 0.4 Pa, while the optimization case of a-IGZO channel deposition was applied for device fabrication in this work. Then, the channel material was annealed by the thermal furnace at 300 °C in the oxygen atmosphere for 30 min. Afterward, in order to achieve a low work function and high conductivity metal contact, the source and drain electrodes were formed by 20-nm thick Ti and 120-nm thick Pt metal film stacks and patterned through the shadow mask with channel width (W) of 500 μm and length (L) of 50 μm. A detailed process flow chart and a three-dimensional (3D) view of the prepared samples are shown in Fig. 1.

Electrical measurements were conducted in the dark chamber at room temperature using Agilent 4156C semiconductor parameter analyzer and 4284A precision LCR meter. Besides, the cross-sectional transmission electron microscope images were taken by JEM-2010F under an operating voltage of 200 kV with the sample prepared by focused ion beam (FEI Helios 1200$^+$, accelerating voltage: 30 kV; ion source: gallium liquid metal). In addition, the chemical bonding states of a-IGZO films were investigated by X-ray photoelectron spectroscopy (XPS). The XPS signal was obtained from a PHI Quantera SXM apparatus from an Al Kα X-ray source operated at 25 W after the sample was sputter-cleaned with an Argon ion beam power and emission current set at 40 W and 4.025 mA, respectively. The binding energy scales of all XP spectra were calibrated by taking the C1s (~284.8 eV) as the reference. The peak fit analysis was performed using the XPSPEAK41 software application. The O1s spectra were fitted to examine the oxygen binding states. Near Gaussian peak shapes were used, the FWHM of the synthetic peak were fixed to 1.5–1.6 eV, and the binding energy of the synthetic peaks were not allowed to change from one spectrum to the other.

3. Results and discussion

Fig. 2 shows the cross-sectional transmission electron microscope images of IGZO TFT with (a) HTS, (b) SHTS and (c) GHTS GI stacks, respectively, while the atomic force microscope images of the interfacial layer and the root-mean-square surface roughness values are also included. The IGZO channel and multilayer gate dielectric are examined by fast Fourier transform, where the diffraction image exhibits the amorphous phases. Besides, a TFT device structure with TaN metal-