



Investigation of low operation voltage InZnSnO thin-film transistors with different high-k gate dielectric by physical vapor deposition

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ABSTRACT

Amorphous Indium-Zinc-Tin-Oxide thin-film transistors (a-IZTO TFT) using different types of high-k materials (like HfO₂, ZrO₂ and Al₂O₃) as gate dielectric are studied in this work. All gate dielectric films were deposited by physical vapor deposition (PVD) process for better composition control. Compared with the traditional SiO₂ gate insulator, a high-k gate dielectric can reduce the operation voltage of TFT device significantly. The TFT device with ZrO₂ gate insulator exhibits a small subthreshold swing of 0.126 V/decade, high field-effect mobility of $\sim 40.7 \text{ cm}^2/\text{Vs}$, low threshold voltage of -0.05 V , and large On/Off current ratio of $\sim 1.01 \times 10^7$. The mechanisms for electrical improvements are also investigated. These results demonstrate the potential application of PVD-deposited ZrO₂ thin film as a promising gate dielectric in oxide-based thin-film transistors.

1. Introduction

During the last decade, amorphous oxide semiconductor thin-film transistor (AOS TFT) was of great interest for applications in the backplane of liquid crystal displays and organic light-emitting diode displays, owing to its excellent electrical performances, low processing temperature, and good uniformity [1–3]. Since Grover firstly reported the amorphous indium zinc tin oxide (a-IZTO) with good field effect mobility in the range of $\sim 15 \text{ cm}^2/\text{Vs}$, a-IZTO has attracted the attention for possible alternative to amorphous InGaZnO (a-IGZO) [4]. Its superior characteristics can be attributed to the better electron conducting path. Under the Madelung potential, the delocalized conduction band minimum (CBM) is mainly constructed by the metal s orbital. Therefore, the non-uniform between cation sites and cation interference might create the fluctuation of CBM, which results in potential barriers against electron transport [5,6]. In contrast, for the a-IZTO material, the unoccupied s-orbital ($4d^{10}5s^0$) of In³⁺ ion and Sn⁴⁺ ion, which may act as the main conducting paths in the channel, have more similar cation sites than In³⁺ ion and Ga³⁺ ion in a-IGZO matrix. As a result, the fluctuation of CBM can be reduced which leading the better electron conducting behavior in this kind of AOS structure [7–9]. Nevertheless, an extremely high conductive channel may easily lead to a nonlinear gate controlled resistor, which may not be depleted by the traditional gate insulator (GI) material in a reasonable gate bias voltage. In the previous work, the precise thermal budget control is needed to avoid

that the devices exhibit all conductive channel [10]. Although some high-k materials, like HfO₂ [11], ZrO₂ [12], Al₂O₃ [13], were proposed to improve the capability of gate control and adjust the negative threshold voltage for the some channel materials. However, the interaction between the a-IZTO channel and different high-k GI materials may be different from other oxide TFTs and the further discussion about the operation mechanisms and bias reliability test are still lacking.

In the present work, three types of high-k material, HfO₂, ZrO₂ and Al₂O₃, are used as the GI layer of a-IZTO TFT for comparisons, in order to achieve a low-voltage operation without performance degradation. Besides, a low-temperature and complete physical vapor deposition (PVD) process was proposed for device fabrication, which may be ideal for large-area display industry and flexible electronics manufacture. Moreover, the mechanisms for electrical improvement are also well discussed in this study.

2. Experiment

TFT devices were manufactured with bottom-gate staggered structure as shown in Fig. 1, which are prepared on doped n-type silicon substrates with 100 nm-thick thermal buffer oxide layer grown on top. Then, a 60-nm-thick TaN thin film was formed and patterned as a gate electrode by direct current (DC) sputtering with a power of 800 W and 100 sccm/10 sccm Ar/N₂ gas flow. After the metal gate electrode formation, a 45-nm-thick GI layer was deposited by electron gun (E-Gun)

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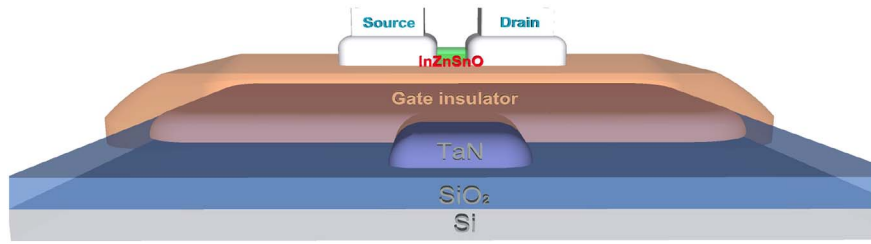


Fig. 1. 3D view of the bottom gate staggered structure in this work.

Table 1

The split table of a-IZTO TFTs with different GI layer in this work.

Sample	HfO ₂	ZrO ₂	Al ₂ O ₃
Substrate	N-type Si with 100 nm thermal SiO ₂		
Bottom gate	60 nm TaN		
Gate insulator	45-nm HfO ₂	45-nm ZrO ₂	45-nm Al ₂ O ₃
High-k PDA	400 °C O ₂ 30 min		
Active layer	20 nm InZnSnO in Ar/O ₂ : 28/2		
Annealing	300 °C O ₂ 20 min		
Source/drain	300 nm Al		

evaporation with HfO₂, ZrO₂, and Al₂O₃, respectively. To further improve the quality of dielectrics film and repair the bulk defects in the GI layer, a post deposition annealing (PDA) was performed at 400 °C in oxygen ambient for 30 min by a thermal furnace after the GI layer deposition. Then, a 20-nm-thick a-IZTO thin film was deposited as the channel layer by RF magnetron sputtering process using a target with the atomic ratio of In:Zn:Sn:O = 4:1:4:15 at room temperature. The optimization condition of a-IZTO channel deposition was applied for device fabrication in this work, in which total gas pressure in the sputter chamber was controlled to be 0.4 Pa, and the flow rate of O₂ and

Ar was set at 2 and 28 sccm, respectively. Then, the a-IZTO channel material was annealed by the thermal furnace at 300 °C in the oxygen atmosphere for 20 min in order to fix the oxygen deficiency in the active layer. Afterward, the source and drain electrodes were formed by using 300-nm-thick Al metal layer with low metal work function and high conductivity contact. All the devices were patterned through the shadow mask with channel width (W) of 500 μm and length (L) of 50 μm. Electrical measurements were conducted in the dark chamber at room temperature using Agilent 4156C semiconductor parameter analyzer and 4284A precision LCR meter. In addition, the chemical bonding states of a-IZTO films were investigated by X-ray photoelectron spectroscopy (XPS). The XPS data was detected and collected by PHI Quantera SXM apparatus with sputtering Argon ion beam, while the power of ion beam and the emission current was set at 40 W and 4.025 mA, respectively. The detailed split table and material structure are shown in Table 1.

3. Results and discussion

Fig. 2(a) shows the drain current versus gate voltage (I_D - V_G) curves of a-IZTO TFTs with different types of GI layers, while the device parameters with an error bar are also summarized in Fig. 2, including

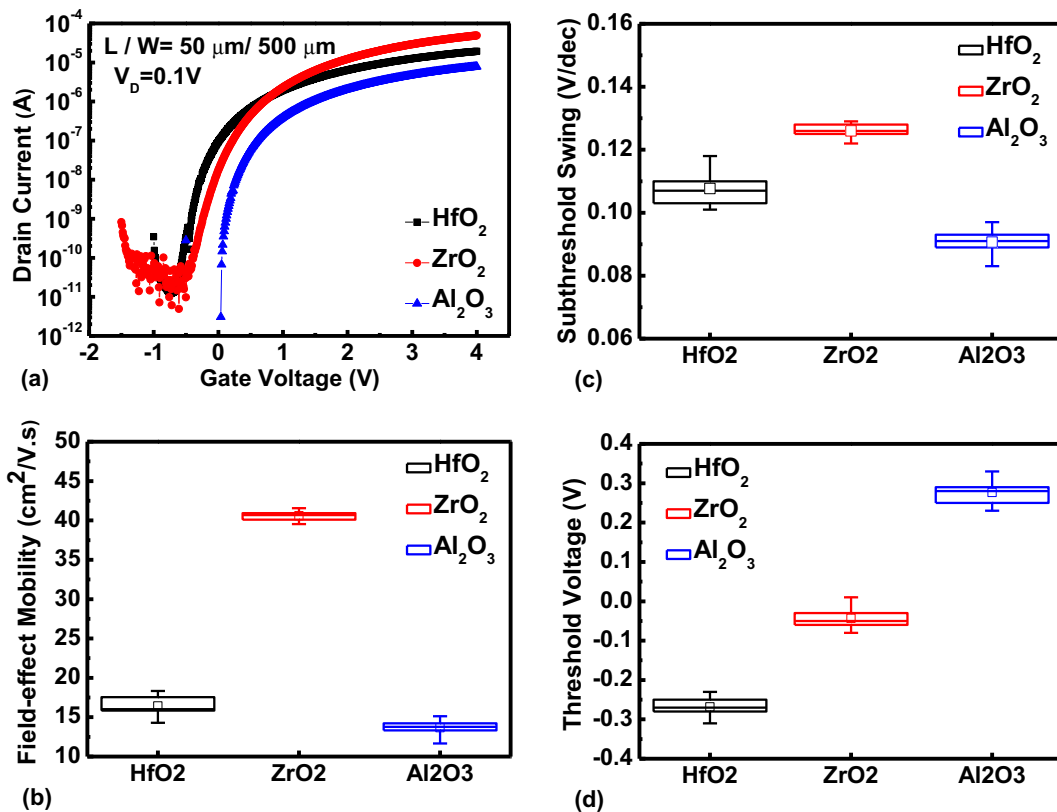


Fig. 2. (a) The I_D - V_G curves of a-IZTO TFTs with different GI layer; the device parameter with error bar for different GI layer, including (b) the field effect mobility (μ_{FE}), (c) the subthreshold swing (S.S.), and (d) the threshold voltage (V_{TH}), each error bar includes six different measuring results for each TFT devices.

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