



Investigation of the degradation mechanisms of silicon thin film anodes for lithium-ion batteries



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ABSTRACT

Silicon is a promising material for negative electrodes in lithium-ion batteries. The degradation of silicon was investigated using thin films between 5 and 50 nm deposited on substrates of varying roughness. We used differential capacity plots to examine the degradation behavior of thin films during cycling. We found that the delamination of the thin films from the substrate depends on the surface roughness and film thickness. The delamination changes the morphology of the thin film and is characterized through the formation of $\text{Li}_{15}\text{Si}_4$. The morphology change is also accompanied by reduced coulombic efficiency and an increasing cell polarization. The transient occurrence of $\text{Li}_{15}\text{Si}_4$ is explained by the processes during cycling. It may be prevented by stress induced potential suppression which was observed in very thin films as the polarization increases with decreasing layer thickness.

1. Introduction

The cycling behavior of silicon is going to play a significant role in future generations of lithium-ion batteries since it is about to enter the market as an additive or replacement for graphite anodes. It is investigated in a variety of morphologies like particles or nanowires [1–4]. At 3759 mAh/g silicon provides ten times the specific capacity of graphite [5]. However, its use is still accompanied with challenges regarding its cycling stability, the most prominent one being the massive volume increase of 270% upon lithiation [6]. As a consequence thereof the electrodes degrade due to a variety of processes [7]. The lithiation leads to mechanical stress inside the active material and results in fracturing. The volume expansion also facilitates the delamination of active layers [8]. Furthermore, it promotes the build-up of the solid electrolyte interphase [9]. These mechanisms are present in electrodes based on particles [10] as well as thin films [11].

In addition to the volume expansion of silicon $\text{Li}_{15}\text{Si}_4$ can be formed during its lithiation. As revealed by XRD studies the initial crystal structure of Si is destroyed during lithiation and turned into amorphous Li_xSi_y [12,13]. Lithiation below 50 mV vs. Li might lead to formation of crystalline $\text{Li}_{15}\text{Si}_4$ [14]. The phase transition during delithiation results in a plateau around 450 mV, comparable to transitions in LFP or LTO [15]. However, the formation of $\text{Li}_{15}\text{Si}_4$ also depends on the thickness of the active layer. Earlier studies suggested that at least 2.5 μm thick layers are necessary to facilitate crystallization of a-Si films to $\text{Li}_{15}\text{Si}_4$ [12]. Recently Iaboni et al. investigated sputtered thin films ranging

from 275 to 1200 nm and cycled using a constant current/constant voltage (CCCV) regime [16] and found that $\text{Li}_{15}\text{Si}_4$ emerges at later cycles and is accompanied by capacity loss and delamination of the thin film. They explained the emergence of $\text{Li}_{15}\text{Si}_4$ as a result of the partial delamination of the thin film from the substrate. However, the expansion of the silicon thin films is hindered through the adhesion to the substrate. The measurements of Sethuraman et al. showed that the resulting stress upon lithiation is capable of reducing the potential by up to 125 mV/GPa and subsequently able to suppress the $\text{Li}_{15}\text{Si}_4$ formation potential [17]. Furthermore, they concluded that Si electrodes deform plastically during cycling. Therefore, high stress may also lead to the delamination of the thin film and thus enable the unimpeded expansion. Subsequently the stress is no longer present during lithiation and $\text{Li}_{15}\text{Si}_4$ is formed. However, no minimal thin film thickness has been demonstrated that would prevent the formation of $\text{Li}_{15}\text{Si}_4$ or the delamination of the active layer.

In this work we investigated the influence of the substrate surface roughness and thin film thickness on $\text{Li}_{15}\text{Si}_4$ formation. Additionally we explored the degradation mechanisms through the cycling behavior of silicon thin films during lithiation. To do so, amorphous Silicon (a-Si) was deposited between 5 and 50 nm using a PECVD process. Differential capacity (dQ/dV) plots provide a useful tool to investigate the processes during cycling and are used to examine the delithiation and lithiation behavior closer. This gives way to an explanation of the emergence and vanishing of $\text{Li}_{15}\text{Si}_4$ during cycling.

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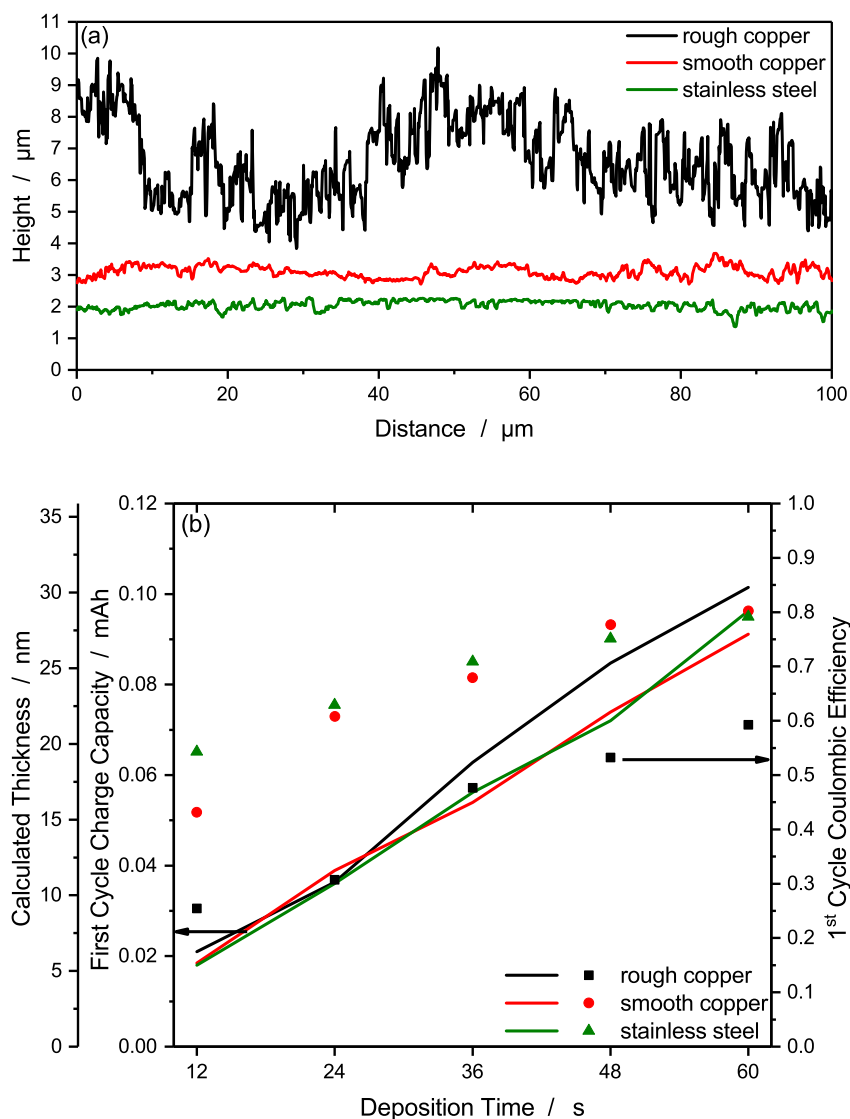


Fig. 1. a) line profiles of the substrate surfaces before a-Si deposition. b) First cycle charge capacity and initial coulombic efficiency of a-Si films on different substrates.

2. Experimental details

2.1. Silicon deposition and characterization

Stainless steel (10 μm thick) (Auerhammer) as well as rough and smooth copper (20 μm) (Schlenk) foils were used as substrates for a-Si thin film deposition that was done simultaneously for all substrates with an Oxford Instruments PECVD System 100 at 1000 mTorr and 250 $^{\circ}\text{C}$. Using a mixture of 25:475 sccm SiH_4 :Ar and 10 W RF resulted in a deposition rate of roughly 25 nm min^{-1} . The anticipated layer thicknesses were 5, 10, 15, 20, 25, and 50 nm. Surface roughness R_a of the substrates was measured with a Keyence VK-9710 laser scanning microscope. SEM pictures were taken with a Phenom ProX located inside an argon filled glove box to omit contamination through moisture or air.

2.2. Pouch cell characterization

Within an argon filled glove box the thin films, cut into $2 \times 2 \text{ cm}^2$ pieces, were assembled into pouch cells with lithium acting as a counter electrode. A mixture of EC:DEC 1:1 with 1 M LiPF_6 and 30% FEC delivered by BASF was used as electrolyte and a sandwich of Celgard 2325

and Whatman filter paper was used as separator. The filter paper served as an electrolyte reservoir and the Celgard faced the silicon electrode to ensure a smooth disassembly for post-mortem investigations. The cells were lithiated using a constant current/constant voltage (CCCV) method down to 10 mV vs. Li^0 with a cut-off current of $2 \mu\text{A cm}^{-2}$ and delithiated with a constant current to 1.5 V vs. Li^0 . The first two cycles were done with $10 \mu\text{A cm}^{-2}$ and the subsequent cycles with $50 \mu\text{A cm}^{-2}$.

3. Results

The line profiles in Fig. 1a illustrate the difference in the surface structure of the substrates. The measured surface roughness R_a of the substrates was 1.0 μm for the rough copper, 0.157 μm for the smooth copper and 0.107 μm for the stainless steel, which was the smoothest substrate in this study.

After a-Si deposition the electrodes were cycled and the first delithiation capacity was used to calculate the thickness of the deposited layer, assuming a specific capacity of 3579 mAh/g and a density of 2.336 g/cm^3 . Fig. 1b shows the first delithiation capacity and the calculated thickness (lines) alongside the coulombic efficiency (dots). Compared to the much smoother substrates, the a-Si layer thickness

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