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Dual-mechanism modelling of instability in nanocrystalline silicon thin film transistors under prolonged gate-bias stress

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ABSTRACT

A dual-mechanism model of the threshold voltage (V_T) shift is proposed for the plasma deposited hydrogenated nanocrystalline silicon (nc-Si:H) thin film transistors (TFTs) stressed under relatively high gate-bias for ~ 10^6 s. ΔV_T versus stress time experimental behavior is modelled by accurate fitting of the combination of stretched exponential and logarithmic dependences. Without such superposition as it is commonly done in other works, i.e. by using any single dependence only, no successful fit was obtained for the V_T shift data at hand. While the stretched exponential behavior is found to be dominant at short stress times, the logarithmic behavior dominates at long stress times. These mathematically distinct behaviors are demonstrated to be attributed to totally distinct TFT instability mechanisms: defect state creation within the nc-Si:H channel layer and charge trapping in the gate insulator. The relaxation data of the stressed TFTs under room temperature support the simultaneous presence of these mechanisms during stressing. In addition, different nanocrystalline volume fractions of the nc-Si:H channel layers of two TFT sets resulted in different ΔV_T versus stress time data, which also supports the dual-mechanism instability model.

1. Introduction

The modern display and large-area sensor technology uses hydrogenated amorphous silicon (a-Si:H) based thin film transistors (TFTs) for switching and in some cases for amplifying/driving each pixel [1–5]. However, the shift of the TFT threshold voltage (V_T) under constant voltage or current make these state-of-the-art devices electrically unstable which necessitates the usage of ΔV_T-compensation pixel circuits to improve TFT stability [5]. This instability issue is undesirable particularly for the amplifying and driving TFT applications respectively in active pixel sensor (APS) X-ray imagers [3, 4] and active matrix organic light emitting diode (AMOLED) displays [5]. The possible instability mechanisms are still under investigation and are not clearly understood. Several different models are proposed to explain this instability phenomenon and to make a lifetime prediction of TFT operation over 10 years or more [6–10]. In addition, to reduce the shift of V_T, it is widely suggested to replace the amorphous TFT channel with the hydrogenated nanocrystalline silicon (nc-Si:H) film [11, 12].

The studies reported on a-Si:H TFT electrical instability usually refer to two mechanisms that are responsible for the shift in V_T under gate-bias stressing: defect state creation mechanism within a-Si:H TFT channel layer close to the semiconductor/insulator interface and charge trapping mechanism within the gate insulator [6]. It is well known that the stress time (t_{stress}) dependence of ΔV_T can be modelled by a stretched exponential behavior for the first mechanism [13], and by a logarithmic behavior for the second mechanism [14]. In some cases, the stretched exponential behavior is also used for the gate insulator charge trapping modelling [10, 15]. Many of the studies model the time dependence of ΔV_T only by one of these behaviors, thus accepting only a single mechanism to be responsible for TFT instability [8, 12, 15, 16]. It is noted that, more or less successful fits of ΔV_T-t_{stress} curve with a single behavior is usually reported for relatively short stress times, i.e. around 10^4 s [7, 8, 11, 12, 17]. However, in some experimental measurements, two separate TFT instability mechanisms are shown to exist together: in [18] at short stress times ΔV_T-t_{stress} has logarithmic behavior attributed to the charge trapping in the gate insulator, whereas at long stress times there is time-dependent trap creation within the a-Si channel. Also recently, a two-stage model has been proposed for ΔV_T-t_{stress} dependence, where two different mechanisms dominate at short ($< 10^3$ s) and long ($> 10^3$ s) stress time values and are modelled by using the same stretched exponential behavior but with different constants [9, 10]. In that model, the initial mechanism responsible for ΔV_T-

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t_{stress} behavior has been attributed to the charge trapping in the gate insulator, which is followed by defect creation inside an a-Si:H channel layer at longer stress times [10]. The literature survey on the electrical instability of nc-Si:H TFTs reveals that under the same stressing conditions, the V_T shift of nc-Si:H TFT is lower compared to that of a-Si:H TFT and usually the stretched exponential expression is used to fit ΔV_T-t_{stress} data [11, 12, 17, 19].

In this work, the shift of transfer curves of two nc-Si:H TFTs with different nanocrystalline volume fractions within the channel layer is measured during relatively high gate-source stressing applied for prolonged stress times up to 10^6 s and followed by relaxation measurements. The positive effect of the nanocrystalline volume fraction on the device stability is shown. However, the main purpose of this study is to present a dual-mechanism model for this shift, where the stretched exponential and the logarithmic dependences are dominant at short and long stress times, respectively. This proposed dual-mechanism instability model is different from the above-mentioned previously reported two-stage models [10, 18] and provides a new insight on the electrical instability mechanisms of nc-Si:H TFT.

2. Experimental part

In this study, two sets of bottom-gate staggered structured TFTs (TFT1 and TFT2) were fabricated in a capacitively coupled PECVD reactor (Plasma Lab μP80, 13.56 MHz) on the chrome (Cr) coated glass substrates by trilayer deposition using a-SiN_x:H as the gate insulator, nc-Si:H as the channel and n^+ nc-Si:H as the ohmic contact layer (Fig. 1). In TFT1 and TFT2, the same growth conditions were used for a-SiN_x:H film deposition: chamber pressure was set to 0.5 Torr, substrate temperature was fixed to 523 K, NH_3/SiH_4 gas flow ratio was set to ~19 and RF power density of 100 mW/cm^2 was utilized. On the other hand, the channel and doped layers of both TFT sets were grown at 473 K and 1 Torr but under different power densities: nc-Si:H/n^+ nc-Si:H films in TFT1 and TFT2 were deposited under 100 mW/cm^2 and 300 mW/cm^2, respectively. Lastly, aluminum (Al) was evaporated above the PECVD grown trilayered structure to be used for the drain (D) and source (S) electrodes. The average thicknesses of all layers for both TFTs are similar and are indicated on the field emission scanning electron microscope (FESEM, Carl Zeiss Ultra Plus Gemini) cross-sectional view of TFT1 in Fig. 1. As it is expected, in the FESEM photograph the gate insulator is dark, while the channel, doped and electrode layers are light, so the nc-Si:H/a-SiN_x:H interface is well distinguished (Fig. 1). To separate TFT devices of the same sample from each other and to pattern D/S electrodes a 2-mask photolithographic method was utilized. To improve the performance of the devices, post-deposition annealing at 423 K for 0.5 h was applied to both TFT sets.

The electrical TFT characterization was done at room temperature by Keithley 230 voltage source and Keithley 617 electrometer. From this current-voltage (*I-V*) characterization, the V_T and other parameters of each TFT were extracted. Then both TFT sets were subjected to the prolonged gate-bias stressing at room temperature and dark conditions via application of high G-S voltages (V_{GS}) without D-S bias (V_{DS}). It was found that V_T of TFT1 is higher than that of TFT2 by ~5 V.

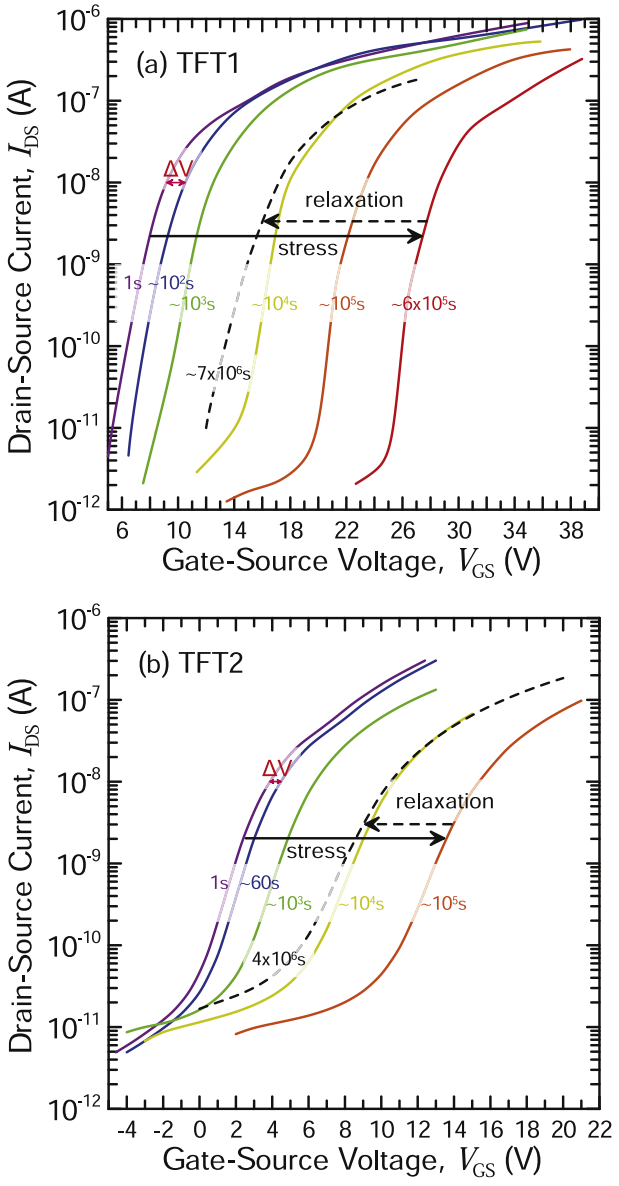

Fig. 2. Demonstration of the shift of the transfer characteristics in the voltage axis presented for various t_{stress} values for (a) TFT1 and (b) TFT2 retrieved at V_{DS} = 1 V during stressing. The last I_{DS}-V_{GS} curve measured during relaxation is also indicated by the dashed line. Note the difference between *x*-axis limits.

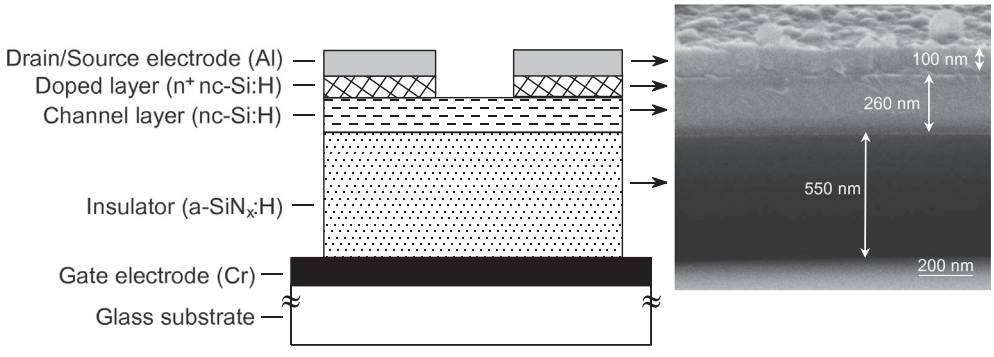

Fig. 1. Schematic representation of the bottom-gate staggered TFT structure of both TFT sets of this study and the corresponding FESEM 50kX magnified cross-sectional image of TFT1.