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Influences of surface treatment on $In_{0.53}Ga_{0.47}As$ epitaxial layer grown on silicon substrate using trimethylaluminum

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ABSTRACT

A development of high quality $In_xGa_{1-x}As$ epitaxial layers on Si substrates is essential for high-performance logic transistors due to the low fabrication cost and high compatibility with a conventional Si technology. We investigate the surface of $In_{0.53}Ga_{0.47}As$ epitaxial layers grown by metal-organic chemical vapor deposition on a Si substrate (with InP/GaAs buffer layers) to obtain a high capacitance using high-k films (HfO_2/Al_2O_3 bilayer). The high-k films were grown on $In_{0.53}Ga_{0.47}As$ epitaxial layers by atomic layer deposition (ALD). The interface between the high-k bilayer and the $In_{0.53}Ga_{0.47}As$ epitaxial layer was analyzed depending on a surface treatment of the $In_{0.53}Ga_{0.47}As$ epitaxial layer, and the surface treatment of the $In_{0.53}Ga_{0.47}As$ epitaxial layer using trimethylaluminum (TMA) enhanced the electrical performances of Pt/high-k film/$In_{0.53}Ga_{0.47}As$ capacitors. The TMA was introduced on the $In_{0.53}Ga_{0.47}As$ epitaxial layer in the ALD chamber, which reduced native oxides (such as gallium and arsenic oxides) of the $In_{0.53}Ga_{0.47}As$ surface and minimized a formation of interfacial layers between the high-k film and $In_{0.53}Ga_{0.47}As$ layer. A capacitance equivalent thickness (CET) of ~1.5 nm was achieved with a low leakage current (~10^{-4} A/cm^2 at 1 V). A CET as low as ~1.3 nm and a capacitance > 2.5 μF/cm^2 was attained by optimizing the high-k/$In_{0.53}Ga_{0.47}As$ interface. The TMA treatment on the $In_{0.53}Ga_{0.47}As$ epitaxial layer is compatible with the conventional Si technology and provides promising opportunities for the development of state-of-the-art field-effect transistor technology using $In_xGa_{1-x}As$ epitaxial layers.

1. Introduction

Compound semiconductors have attracted significant attention over the past few decades due to their high carrier mobility that enables the fabrication of high-performance metal-oxide-semiconductor field effect transistors with capabilities beyond those obtained using conventional Si as a channel material [1–8]. GaAs and $In_xGa_{1-x}As$ are representative materials with a high electron mobility (> 5000 cm^2/Vs) [3]. An InP substrate is typically grown by molecular beam epitaxy and used to grow the $In_xGa_{1-x}As$ layers by metal-organic chemical vapor deposition (MOCVD). However, InP substrates are fragile and have a high production cost; which is inappropriate for a mass-production [9]. In this respect, hetero-epitaxial compound semiconductors grown on Si substrates have received considerable interest which is compatible with the state-of-the-art field-effect transistor technology compared to lattice-matched substrates [9,10]. To grow $In_xGa_{1-x}As$ epitaxial layers on a Si substrate, InP/GaAs layers are typically deposited as buffer layers by MOCVD to minimize a lattice mismatch between the $In_xGa_{1-x}As$ layer and the Si substrate [9,11,12]. Lin et al. reported that the thickness of InP/GaAs buffer layers could be as low as 0.84 μm for the growth of $In_xGa_{1-x}As$ layer, with a low interface trap density (D_{it}). However, the capacitance equivalent thickness (CET) was higher than 3.5 nm with a capacitance lower than 1 μF/cm^2 using Al_2O_3 as a high-k film [9]. A CET of 0.9 nm was recently reported using an $In_xGa_{1-x}As$ epitaxial layer grown on a Si substrate with InAlAs/InP/GaAs buffer layers [13]. For an achievement of high capacitance density, surface treatments on $In_xGa_{1-x}As$ epitaxial layers were attempted using HF, $(NH_4)_2S$, and trimethylaluminum (TMA) [14–21]. It was reported that HF solution eliminated native oxides on III-V materials, generating temporary hydrogen-passivated surfaces [14]. The

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treatment using $(NH_4)_2S$ was effective in the removal of native oxides on III-V surfaces which was replaced by one or two monolayers of sulfur [16], however, small amount of native oxides remained on the III-V surface which degraded electrical performances of III-V materials. A surface treatment using TMA has been reported for GaAs-based materials via oxygen scavenging effect on GaAs surfaces, however, the removal of native oxides was not sufficient by TMA alone [18–21]. Despite of the research on III-V surface treatments, the detailed analysis in the elimination of native oxides and interfacial layers between high-k film and $In_xGa_{1-x}As$ epitaxial layer grown on a Si substrate has not been systematically studied.

In this work, we investigate the interface of the high-k film/$In_{0.53}Ga_{0.47}As$ layer to achieve a high capacitance density (> 2.5 μF/cm^2). The $In_{0.53}Ga_{0.47}As$ epitaxial layers were grown on the Si substrate via MOCVD using InP/GaAs buffer layers, and the high-k films were grown on $In_{0.53}Ga_{0.47}As$ layers by atomic layer deposition (ALD). A surface treatment of the $In_{0.53}Ga_{0.47}As$ layer was performed in the ALD chamber using TMA to remove native oxides on the $In_{0.53}Ga_{0.47}As$ surface and minimize a formation of interfacial layer at the high-k film/$In_{0.53}Ga_{0.47}As$ interface. With the effect of TMA, electrical properties of the Pt/high-k film/$In_{0.53}Ga_{0.47}As$ capacitors were enhanced significantly. A CET below ~1.5 nm was achieved with a low-leakage current (~10^{-4} A/cm^2 at 1 V) for Pt/high-k film (HfO_2/Al_2O_3)/$In_{0.53}Ga_{0.47}As$ capacitors. A CET as low as ~1.3 nm was achieved by optimizing the high-k/$In_{0.53}Ga_{0.47}As$ interface, and the resultant high capacitance has rarely been reported using $In_xGa_{1-x}As$ epitaxial layers grown on the Si substrate [13].

2. Experimental

A 506-nm-thick $In_{0.53}Ga_{0.47}As$ epitaxial film was grown by MOCVD (Aixtron Crius) on an InP(1073 nm)/GaAs(536 nm)/Si substrate at 550 °C. A 6° off-cut Si substrate [6 in., (001), 6° tilt] was used as the base substrate on which the InP and GaAs buffer layers were grown to minimize the lattice mismatch. The InP/GaAs buffer layers were deposited on the Si substrate at 450 °C for the subsequent growth of the $In_{0.53}Ga_{0.47}As$ epitaxial layer. Trimethyl-gallium and trimethyl-indium were used as the gallium and indium precursors, respectively, with H_2 carrier gases. AsH_3 and PH_3 were used as the arsenic and phosphor precursors, respectively.

The $In_{0.53}Ga_{0.47}As$ surface was cleaned by submersion in a HCl (20%) solution to remove organic compounds from the $In_{0.53}Ga_{0.47}As$ surface [22]. An $(NH_4)_2S$ solution was used to remove the native oxides from the $In_{0.53}Ga_{0.47}As$ surface. The $In_{0.53}Ga_{0.47}As$ samples were submerged in $(NH_4)_2S$ (20%):H_2O = 1:1 for 20 min at room temperature and then rinsed with H_2O [17,22–26]. All $In_{0.53}Ga_{0.47}As$ samples were submerged in $(NH_4)_2S$ solution for sulfur treatment to reduce the native oxide from the $In_{0.53}Ga_{0.47}As$ surface before the growth of high-k films by ALD. Electrical and chemical properties of $In_{0.53}Ga_{0.47}As$ samples without and with the TMA treatment were compared to verify the influence of TMA on the $In_{0.53}Ga_{0.47}As$ layer. For the TMA treatment, TMA molecules were introduced to the $In_{0.53}Ga_{0.47}As$ samples for 4 s in the ALD chamber at 200 °C before the deposition of the HfO_2/Al_2O_3 films by ALD.

Al_2O_3 films were deposited by ALD on $In_{0.53}Ga_{0.47}As$ layers using TMA and H_2O as the Al precursor and oxygen source at a growth temperature of 200 °C. The ALD sequence consisted of TMA pulse (0.6 s)/purge (11 s)/H_2O pulse (0.6 s)/purge (10 s) steps. HfO_2 films were grown by ALD using tetrakis(ethylmethylamino)hafnium {Hf[N(CH_3)C_2H_5]$_4$} as the Hf precursor and H_2O as the oxygen source at a growth temperature of 200 °C.

X-ray diffraction (XRD, Bruker, D8 Discover) with θ–2θ and rocking mode was used to analyze the crystallinity of the $In_{0.53}Ga_{0.47}As$ epitaxial layer and InP/GaAs buffer layers. The crystallinity was also investigated by high-resolution transmission electron microscopy (HR-TEM, JEOL, JEM-2100F) with a selected area electron diffraction (SAED) mode. The operation voltage was 200 kV. The sample was prepared using a focused ion beam (FEI, NOVA 600 Nanolab) with a Pt passivation layer. The chemical nature of the $In_{0.53}Ga_{0.47}As$ was analyzed by X-ray photoelectron spectroscopy (XPS, ThermoVG SIGMAPROBE) using monochromatic Al K_α radiation without Ar sputtering on sample surfaces.

The Pt/high-k film/$In_{0.53}Ga_{0.47}As$ capacitors were fabricated for analyzing their electrical properties. An In metal was used to achieve an ohmic contact with the $In_{0.53}Ga_{0.47}As$ layer. A 50-nm-thick Pt electrode was deposited as a top electrode by e-beam evaporation using a circular-patterned shadow mask (diameter of 150 μm). The samples were annealed in the forming gas (H_2 5%, N_2 95%) ambient at 300 °C for 0.5 h in a typical tube furnace. The capacitance-voltage (C-V) characteristics were measured using Keithley SCS 4200 parameter analyzer with the C_s-R_s series equivalent circuit model. Current-voltage (I-V) curves were obtained using the HP4155 semiconductor parameter analyzer. CET was calculated from the accumulated capacitance measured at 1 MHz.

3. Results and discussion

Fig. 1(a) shows a θ–2θ XRD pattern of the $In_{0.53}Ga_{0.47}As$ epitaxial layer grown on the Si substrate by MOCVD using InP/GaAs buffer layers [$In_{0.53}Ga_{0.47}As$(506 nm)/InP(1073 nm)/GaAs(536 nm)/Si stack is shown in Fig. 1(c)]. A peak at 63.37° corresponded to the (400) InGaAs/InP layers, and a peak at 66.23° originated from the (400) GaAs layer. Threading dislocation density was estimated to be 5.8×10^9 cm^{-2} from the full width half maximum (FWHM) of InGaAs/InP rocking curve using the Ayers model, as shown in Fig. 1(b) [27]. Fig. 1(c) presents the cross-sectional TEM image of the $In_{0.53}Ga_{0.47}As$/InP/GaAs/Si substrate. Fig. 1(d)–(g) present diffraction patterns from the Si substrate, GaAs, InP, and InGaAs layers obtained from the TEM with a SAED mode. The electron diffraction pattern consisted of single spots, indicating a high-quality $In_{0.53}Ga_{0.47}As$ epitaxial layer with InP/GaAs buffer layers grown on the Si substrate. The $In_{0.53}Ga_{0.47}As$ epitaxial layer was n-type with an electron concentration of ~8×10^{17}/cm^3 and an electron mobility of ~8180 cm^2/Vs at room temperature (by Hall measurement, not shown here).

Fig. 2(a) and (b) present frequency-dependent C-V curves from Pt/HfO_2(4 nm)/Al_2O_3(~1 nm)/$In_{0.53}Ga_{0.47}As$ capacitors without and with the TMA treatment on $In_{0.53}Ga_{0.47}As$ layers before the growth of HfO_2/Al_2O_3 films by ALD. The sample without TMA treatment of the $In_{0.53}Ga_{0.47}As$ layer exhibited a larger frequency dependence of capacitance in the depletion region compared to that of the TMA-treated sample. This result implies that the TMA treatment reduced interface defects (near the valence band edge) formed by dangling bonds, native oxide, and interfacial layers [17,28–31]. TMA has been reported to facilitate oxygen atom scavenging on diverse oxide surfaces [18–20]. It is anticipated that the native oxides on the $In_{0.53}Ga_{0.47}As$ layer are eliminated by the TMA treatment. Oxygen scavenging in native oxides on the $In_{0.53}Ga_{0.47}As$ surface was viable by the TMA treatment because of a formation of a strong bond between Al and O as reported elsewhere [18–21]. In the meantime, severe distortion in the C-V curve was observed in Fig. 2(a), which hardly exhibited the accumulation of carriers at lower frequencies (< 100 kHz) in the accumulation region (> 1 V). The distortion in the C-V curve at a lower frequency originated from a large leakage current at high positive voltages. The leakage current contributed to increase in capacitance in a C_s-R_s series equivalent circuit model, which was supported by I-V curve (Fig. 2(c)). However, the distortion in the C-V curve was substantially suppressed by the TMA treatment of $In_{0.53}Ga_{0.47}As$, as shown in Fig. 2(b), due to the decreased leakage current (Fig. 2(c)). The lower leakage current of the $In_{0.53}Ga_{0.47}As$ sample under TMA treatment was attributed to reduced defects on the TMA treated-$In_{0.53}Ga_{0.47}As$ layer in which a trap-related conduction mechanism was involved [17,24–26].

The elimination of native oxides by the TMA treatment on the