Transport property improvements of amorphous In–Zn–O transistors with printed Cu contacts via rapid temperature annealing

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ARTICLE INFO

ABSTRACT

The device performance of amorphous In–Zn–O (a-IZO) thin-film transistors (TFTs) with printed Cu contacts was significantly improved by the insertion of a diffusion barrier Ta layer and rapid thermal process (RTP) annealing. Furnace-annealed a-IZO TFTs with Cu/Ta contacts exhibited mobility values of 21.3 cm^2/Vs, subthreshold gate swing (SS) values of 1.9 V/decade, and $I_{ON/OFF}$ of ~10^6. In contrast, the SS, mobility, and $I_{ON/OFF}$ ratio of RTP-annealed a-IZO TFTs with Cu/Ta contacts were 30.6 cm^2/Vs, 0.68 V/decade, and 3 × 10^7, respectively. We attributed the performance improvement of devices with Cu/Ta contacts to the suppression of Cu in-diffusion within the a-IZO channel due to the rapid heating associated with RTP annealing.

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1. Introduction

Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) are widely used as pixel drivers for advanced active-matrix liquid crystal displays and organic light-emitting displays due to reasonable mobility values of ~10 cm^2/Vs, good substrate size scalability, and extremely low leakage currents [1–2]. The RC delay time for backplane electronics must be aggressively reduced to meet the current stringent requirements for high pixel densities (≥2000 × 4000), high frame rates (≥240 Hz), and 3-dimensional visual effects [3]. With this regard, high-speed AOS transistors with low resistivity wiring interconnections are being intensively investigated. Cu interconnections compatible with AOS thin-film transistors (TFTs) are highly desirable due to the low resistivity of Cu (1.68 μΩ cm). However, the migration of Cu atoms into the AOS layer during contact annealing serves to degrade transfer characteristics [4–5]. Therefore, diffusion barriers such as titanium (Ti) [6], molybdenum (Mo) [7], tantalum (Ta) [8], and molybdenum titanium (MoTi) [9] are being used in TFTs with Cu contacts.

Thus far, Cu films as contact layers for TFTs have been primarily prepared via expensive vacuum-based sputtering deposition methods [4–10]. On the other hand, solution-based processes may reap potential benefits such as simplified processes, low costs, and high throughput. Despite these benefits, the use of printed Cu films as contact layers in AOS TFTs has been limited due to the difficulty of proper ink formation and the anti-oxidation of Cu films during thermal annealing [11–12]. Furthermore, few studies have investigated which diffusion barriers and contact annealing processes are most optimal for AOS TFTs.

In this study, we report on the device performance of a-IZO TFTs with reverse offset printed Cu contacts. To suppress Cu diffusion into the a-IZO channel during contact annealing, rapid thermal processing (RTP) and Ta layer diffusion barrier insertion were employed. Furnace annealing of a-IZO TFTs with Cu/Ta contacts resulted in TFTs with reasonable transport properties. However, RTP-annealed a-IZO TFTs exhibited superior mobility values (μ_{FE}), smaller subthreshold gate swing (SS) factors, and larger $I_{ON/OFF}$ ratios than furnace-annealed a-IZO TFTs. The μ_{FE}, SS, threshold voltage (V_{TH}), and $I_{ON/OFF}$ ratios of RTP-annealed devices were 30.6 cm^2/Vs, 0.68 V/decade, 1.0 V, and 3 × 10^7, respectively. We determined reasons for these improvements based on Cu distribution profiles and contact resistance analysis.

2. Experimental

A 100-nm-thick SiO$_2$ layer was grown via thermal oxidation and a heavily doped p-type Si wafer was used as the gate electrode. A 28 nm thick IZO film (AOS channel) was prepared for bottom gate TFTs via magnetron sputtering of the SiO$_2$/Si substrate with In:Zn at an atomic ratio of 6:4. The distance between the IZO substrate and target was ~16 cm and the DC sputtering power was fixed to 100 W. The working pressure was 0.26 Pa and the relative oxygen ratio ([O$_2$]/[Ar + O$_2$]) was

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0.30. A 10 nm thick Ta diffusion barrier layer was deposited via DC sputtering onto the IZO/SiO$_2$/Si substrate. A Cu film source/drain (S/D) electrode was prepared via low-cost reverse offset printing. Cu inks were obtained from Dongjin SemiChem. Inc.; these inks consisted of Cu nanoparticles, binders, additives, and solvents. The Cu ink mass density and wt.% of Cu nanoparticles within the Cu ink were 1.21 g/ml and 44.1%, respectively. Cu films as the S/D electrode were prepared via reverse offset processes [13]. Cu inks were coated onto a blanket and then transferred to the cliché by rolling with an inverse S/D pattern. The cliché, which removed unnecessary parts on the blanket, was made from a 100 μm thick stainless steel foil. The remaining S/D pattern on the blanket was manually printed onto the IZO/SiO$_2$/Si substrate. The printed Cu film was sintered in a furnace for 10 min at 250 °C under an ambient N$_2$ atmosphere. The ramp rate of the furnace was approximately 5 °C/min. To effectively reduce the sintering time, RTP annealing was also carried out. The annealing conditions used for RTP were the same as those used for furnace annealing with the exception of the ramp rate (60 °C/min). The physical thickness of the printed Cu film onto the IZO/SiO$_2$/Si substrate was approximately 1.3 μm, irrespective of the sintering methods. The contact resistance of both device types was determined using the transmission line method (TLM). Devices with channel lengths of 100, 150, 200, and 250 μm were used for TLM analysis. Transfer characteristics of the a-IZO TFTs were measured at room temperature using a Keithley 2636 source meter. The thickness of the ZTO channel layer and Cu film was evaluated by ellipsometry (K-Mac, STER) and scanning electron microscopy (SEM, Hitachi, S-4300), respectively, which was confirmed by cross-sectional transmission electron microscopy (XTEM, FEI, Tecnai F20) operating at 200 kV. The crystalline quality of Cu films was analyzed by theta/2theta X-ray diffraction (XRD, PANalytical, X'Pert-PRO,) using Cu Kα radiation operating at 40 kV. Cu depth profiles for the Cu/Ta/IZO stacks were examined via XTEM and energy dispersive X-ray spectroscopy (EDS).

3. Results and discussion

Fig. 1a and b shows the SEM images of the furnace- and RTP-annealed printed Cu films on the SiO$_2$/Si substrate, respectively. Both films exhibited well-dispersed spherical morphologies, suggesting that Ostwald ripening-induced sintering occurred during the annealing process. Peaks at 43.3, 50.5, and 74.2° in the X-ray diffraction patterns for both films were identified as Cu (111), (200), and (220) reflections,

respectively (Fig. 1c) [14]. No copper oxide peaks were detected in either film type. Cu grain coalescence was more pronounced in the furnace-annealed Cu films over the RTP-annealed films, which was attributed to a higher thermal budget for furnace-annealing due to a lower ramp rate.

Fig. 2a and b presents the representative transfer characteristics of furnace- and RTP-annealed a-IZO TFTs, respectively. The μ_{FE} was determined by the maximum transconductance at a drain voltage (V_{DS}) of 0.1 V. The V_{TH} was determined by the gate voltage (V_{GS}), which induced a drain current of L/W × 10 nA at a V_{DS} of 5.1 V. The SS ($SS = dV_{GS}/dlogI_{DS}$ [V/decade]) was extracted from the linear component of the log(I_{DS}) vs. V_{GS} plot. The bulk trap density (N_{SS}) of the TFTs was calculated from the following equation: $SS = qk_BT \cdot N_{SS}t_{ch}/[C_i\log(e)]$, where q is the charge of an electron, k_B is Boltzmann's constant, T is the absolute temperature, and t_{ch} is the channel layer thickness [15]. The furnace-annealed device exhibited a μ_{FE} value of 21.3 ± 5.0 cm^2/Vs, SS of 1.88 ± 0.4 V/decade, V_{TH} of 5.5 ± 1.0 V, and an $I_{ON/OFF}$ ratio of 1 × 10^6. By contrast, the RTP-annealed a-IZO TFTs exhibited a μ_{FE} of 30.6 ± 4.0 cm^2/Vs, SS of 0.68 ± 0.2 V/decade, V_{TH} of 3.4 ± 1.0 V, and $I_{ON/OFF}$ ratio of 3 × 10^7. It was noted that non-negligible variations in the μ_{FE}, SS, and V_{TH} values of the a-IZO TFTs were due to manual printing of the S/D pattern blanket onto the IZO/SiO$_2$/Si substrate. The μ_{FE} values reported for AOS TFTs with printed Cu and lacking a diffusion barrier were limited to 0.4–1.4 cm^2/Vs [11–12]. Therefore, the high μ_{FE} values (21.3–30.6 cm^2/Vs) in this study could be attributed to both the adoption of proper Ta diffusion barriers and the low effective electron mass of the a-IZO films, which were comparable or superior to those of AOS TFTs (4.8–18.7 cm^2/Vs) with vacuum-based Cu contacts [5–10]. Contact resistance (R_C) values for the furnace- and RTP-annealed devices were approximately 212 and 103 Ω cm, respectively, as determined via TLM analysis shown in Fig. 3. R_C corrected intrinsic channel mobility ($\mu_{intrinsic}$) values for thermally-annealed and RTA-treated TFTs were 31.0 and 35.3 cm^2/Vs, respectively. This indicated that higher μ_{FE} values for the RTP-annealed a-IZO TFTs over the furnace-annealed a-IZO TFTs were due to the lower R_C values of the former devices. The superior μ_{FE} values of the RTP-annealed a-IZO TFTs were reflected in high I_{DS} levels (Fig. 2d) compared with those of furnace-annealed a-IZO TFTs (Fig. 2c).

In-diffusion of Cu impurities into the underlying a-IZO channel layer through the Ta diffusion layer was analyzed via EDS. Fig. 4 presents cross-sectional TEM images for the furnace- and RTP-annealed Cu/Ta/
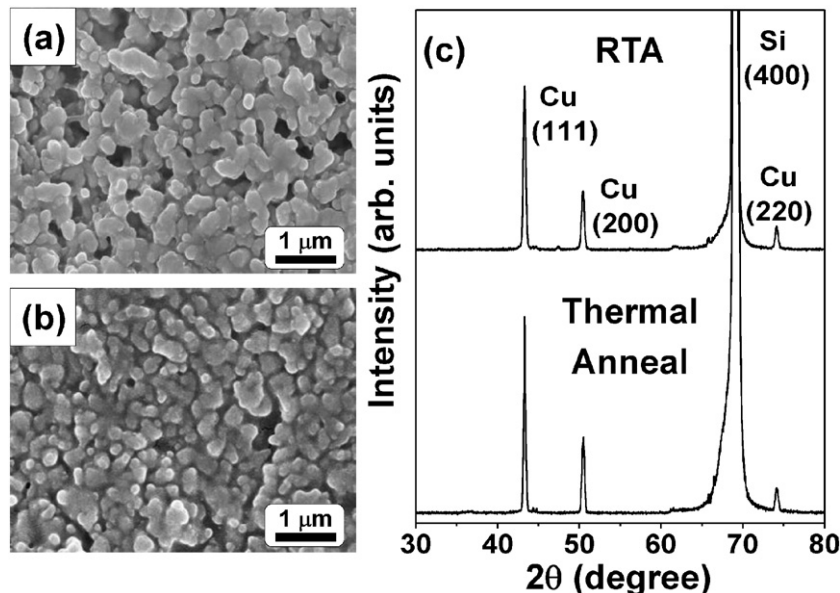

Fig. 1. SEM images of (a) furnace- and (b) RTP-annealed printed Cu films on SiO$_2$/Si substrates. (c) XRD patterns of both Cu films.