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Misorientation dependent epilayer tilting and stress distribution in heteroepitaxially grown silicon carbide on silicon (111) substrate

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ABSTRACT

The advantages and disadvantages of using off-axis substrates for heteroepitaxial growth of 3C-SiC on Si(111) substrates are investigated in this paper. 3C-SiC is deposited on on-axis and 4° off-axis 150 mm Si(111) substrates using low pressure chemical vapour deposition. The dependence of surface morphology, roughness, crystallinity, alignment between the epilayer and the substrate, and film stress are evaluated using atomic force microscopy, X-ray diffraction, and wafer curvature measurement. Highly parallel steps are observed on both on-axis and off-axis Si substrates after surface preparation, yet step density is doubled and step height is much larger (>21 times of single step height) for 4° off-cut Si compared to on-axis Si. X-ray diffraction results indicate that SiC grown on on-axis Si substrates are well-aligned with the Si substrates, while the SiC grown on off-axis substrates are tilted positively by as large angle as 1.66°. The well-aligned SiC grown on on-axis Si substrate exhibits lower and uniform residual stress compared to the film grown on off-axis Si substrates, which exhibits a nonuniform distribution of higher stress. The stress distribution is found to be dependent on Si surface step direction and height. These misorientation dependent tilting and stress distribution mechanisms are expected to be applicable to other hetero-epitaxial growth systems with similar mismatch magnitude.

1. Introduction

SiC has a wide energy gap and excellent physical, electrical, and chemical properties. SiC has more than 200 different polytypes, amongst them, 3C-SiC is the only SiC polytype that can be grown on large-diameter, low cost Si substrates. It offers the potential of integrating SiC-based electronics with mature Si technology and the 3C-SiC/Si structure can act as an excellent cost-effective template for graphene preparation [1,2]. In addition, as the research interest for fabrication of GaN-based blue light-emitting diodes is soaring up, the use of 3C-SiC/Si(111) template for GaN growth shows great potential for reducing the intrinsic strain, improving crystal quality and obtaining large-area crack-free GaN films [3–6]. Consequently, there is a great need for an in-depth investigation of parameters that exert impacts on the properties of the grown 3C-SiC. Relatively extensive investigations had been performed for the growth of 3C-SiC on on-axis Si(111) substrates, yet very limited knowledge and information are available in the open literature for the growth of 3C-SiC on off-oriented Si(111) substrates. It was shown that the surface roughness, stacking fault density, and stress magnitude were heavily dependent on the off-cut direction, where a smoother SiC film with lower stress magnitude and less stacking fault density was achieved on off-axis Si substrate tilted towards [110] direction as compared with [112] direction [7,8]. Therefore, the merit of using either on-axis or off-axis substrates must be evaluated on a case-by-case basis. Although the differences in surface morphology, roughness, stress, and crystalline quality had been reported for the growth of 3C-SiC on off-oriented Si, the root cause of them has not been investigated. In addition to that, tilting/inclination of the grown epitaxial layer relative to the substrate has been widely reported for hetero-epitaxial growth of other different materials [9–12], however, there is no investigation that had been performed to evaluate the tilting degree of the hetero-epitaxially grown 3C-SiC film. Therefore, in this paper, we present a comprehensive study of the impact of the Si substrate misorientation on the surface morphology, crystal quality and orientation, and stress of deposited 3C-SiC using atomic force microscopy (AFM), X-ray diffractometry (XRD), and wafer curvature and stress measurements. Also, a mechanism for the observed misorientation-dependent properties of the grown SiC is proposed.

2. Experimental details

The growth of 3C-SiC was performed on both on-axis (off-cut angle $<$ 0.5°) and off-axis (off-cut angle of 3.5 ± 0.5° towards [110]) 150-mm Si(111) substrates (both are p-type doped with resistivity in the range of 1–10 Ω · cm) using a custom-made low-pressure chemical vapour deposition reactor at a temperature of 1000 °C. Si wafers were loaded into the reactor at 600 °C as received (without pre-treatment). The

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temperature was ramped up at a rate of 5 °C/min under oxygen (100 sccm (standard cubic centimetre per minute)) in a pressure of 95 Pa to maintain the native oxide on the Si surface, which minimises the risk of carbon contamination of the silicon surface prior to a SiH_4 oxide removal process. The native oxide formed on the Si substrate surface was removed using low pressure SiH_4 at 1000 °C to ensure a sharp 3C-SiC/Si interface. Following the removal of oxide, continued SiH_4 flow grows a fresh layer of Si on the activated Si substrate. This is then followed by a carbonisation step performed at 750 °C to convert the clean Si surface into SiC layers. Epitaxial growth was then subsequently initiated at 1000 °C using alternating supply epitaxy with SiH_4 and C_3H_6 as precursors. The details of this growth procedure are reported in refs. [13,14].

XRD measurements were performed with a Panalytical Empyrean X-ray diffractometer, with a high resolution four-crystal Ge (220) asymmetrical incident beam monochromator, using Cu $K\alpha 1$ radiation ($\lambda = 1.5405980$ Å), and a PIXcel-3D detector with a fixed anti-scatter slit. The PIXcel detector is used in the Open Detector (OD) mode for the rocking curve and phi scan measurements. AFM measurements were performed using Park NX20 under non-contact mode. Cross-section transmission electron microscopy (TEM) characterisation was performed using FEI Tecnai F20 TEM (operating at an accelerating voltage of 200 keV). SiC cross-sectional slices were diced using diamond saw along the $[\bar{1}\bar{1}2]$ direction, they were thinned down using sandpaper and finally by precision ion polishing system. The incident beam during TEM observation was injected along $[\bar{1}10]$ direction. Due to excellent wafer thickness uniformity achievable with our optimised process (better than 99% uniformity across 150-mm wafer), a Tencor Flexus 2320 system was used for monitoring wafer curvature prior to and after epitaxial growth. The scans were done along the diameter of 150 mm wafers with 10 mm edge exclusion. The biaxial stress for SiC films was calculated on the basis of the modified Stoney's equation [15–17], using the appropriate elastic moduli (E) and Poisson's ratio values: 170 GPa and 0.26 for Si(111).

3. Results and discussion

3.1. The morphology and roughness

Substrate surface morphology plays a very important role in the kinetics of epitaxy process and significantly impacts the crystalline quality of the grown film. The surface morphology and root-mean-square (RMS) roughness of Si substrates after in-situ surface preparation and grown SiC films at different process stages were characterised using AFM and are shown in Figs. 1 to 3.

Fig. 1(a) shows the presence of step-like features on the on-axis Si surface after the in-situ Si surface cleaning using $SiH_{4,}$ with root mean square RMS roughness of ~0.17 nm over 1 μm × 1 μm scan area. The origin of the small particulates that are evenly populating the surface is unclear and under current investigation. The terrace width ranges from ~155 to ~322 nm with an average step height of 0.31 nm, shown in Fig. 1(b), indicating that a single step on Si(111) corresponds to double layers of Si atoms [18]. The calculated off-cut angle is therefore less than 0.1°, and no obvious step-bunching phenomenon was observed. The off-cut angle of the on-axis Si wafer was measured by XRD to be 0.06°, in a good agreement with AFM results and supplier specification. In contrast, Fig. 1(c) shows that the in-situ cleaned off-axis Si wafer had a much larger RMS roughness of 1.55 nm. Highly parallel steps along $[\bar{1}10]/[1\bar{1}0]$ direction have been observed on off-oriented Si substrates, the steps are normal to the wafer primary flat. From Fig. 1(d), it is clearly shown that the step density is twice as high as the step density on the on-axis wafer, with step spacing ranged from ~82 nm to ~117 nm and step height varied from 6.67 nm to 8.33 nm, which is more than 21 times higher than the step formed on on-axis Si. Its terrace width and step height are very similar to what has been reported for 4° off-cut Si(111) towards [110] [19], whose component vector in the (111) plane is pointing in $[11\bar{2}]$ direction. XRD measurement also confirmed that the off-cut angle of the off-axis Si wafer is ~4.0°. Fig. 1(c) and (d) clearly demonstrates that step

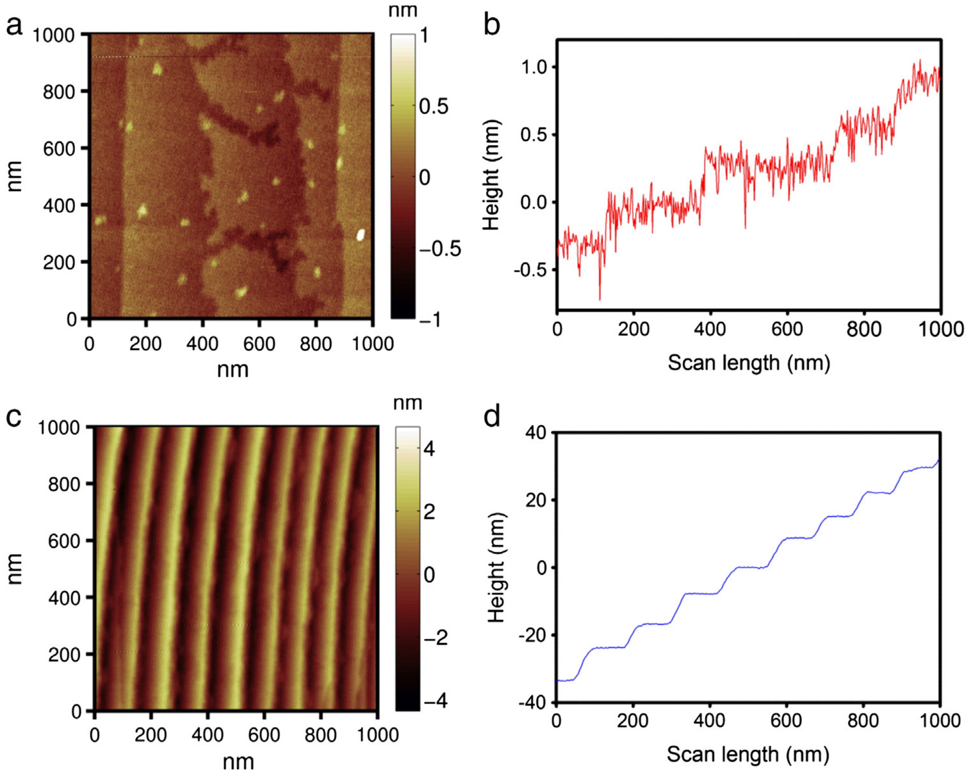

Fig. 1. Top-view AFM images and surface line profile of Si surface after in-situ cleaning: (a) top-view morphology of on-axis Si, (b) surface line profile of on-axis Si, (c) top-view morphology of ~4.0° off-axis Si, and (d) surface line profile of ~4.0° off-axis Si. The scan area is 1 μm × 1 μm.

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