Thin Solid Films 557 (2014) 42–49

Contents lists available at ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

3D heteroepitaxy of mismatched semiconductors on silicon

Claudiu V. Falub [a,*], Thomas Kreiliger [a], Fabio Isa [b], Alfonso G. Taboada [a], Mojmír Meduňa [c,d], Fabio Pezzoli [e], Roberto Bergamaschini [e], Anna Marzegalli [e], Elisabeth Müller [f], Daniel Chrastina [b], Giovanni Isella [b], Antonia Neels [g], Philippe Niedermann [g], Alex Dommann [g,1], Leo Miglio [e], Hans von Känel [a]

[a] Laboratory for Solid State Physics, ETH-Zürich, Schafmattstrasse 16, 8093 Zürich, Switzerland
[b] L-NESS, Department of Physics, Politecnico di Milano, via Anzani 42, 22100 Como, Italy
[c] Department of Condensed Matter Physics, Masaryk University, Kotlářská 2, 61137 Brno, Czech Republic
[d] CEITEC, Masaryk University, Kamenice 5, 60177 Brno, Czech Republic
[e] L-NESS, Department of Materials Science, Università degli studi di Milano-Bicocca, via Cozzi 53, 20125 Milano, Italy
[f] Electron Microscopy ETH-Zürich (EMEZ), Schafmattstrasse 16, 8093 Zürich, Switzerland
[g] Centre Suisse d'Electronique et Microtechnique, Jaquet-Droz 1, 2002 Neuchatel, Switzerland

ARTICLE INFO

Available online 28 October 2013

Keywords:
Monolithic integration
Epitaxial growth
Ge
GaAs
Patterned Si substrates
Scanning X-ray nano-diffraction
Room-temperature photoluminescence
X-ray detectors

ABSTRACT

We present a method for monolithically integrating mismatched semiconductor materials with Si, coined three-dimensional (3D) heteroepitaxy. The method comprises the replacement of conventional, continuous epilayers by dense arrays of strain- and defect-free, micron-sized crystals. The crystals are formed by a combination of deep-patterning of the Si substrates and self-limited lateral expansion during the epitaxial growth. Consequently, the longstanding issues of crack formation and wafer bowing can be avoided. Moreover, threading dislocations can be eliminated by appropriately choosing pattern sizes, layer thicknesses and surface morphology, the latter being dependent on the growth temperature. We show this approach to be valid for various material combinations, pattern geometries and substrate orientations. We demonstrate that Ge crystals evolve into perfect structures away from the heavily dislocated interface with Si, by using a synchrotron X-ray beam focused to a spot a few hundred nanometers in size and by recording 3D reciprocal space maps along their height. Room temperature photoluminescence (PL) experiments reveal that the interband integrated PL intensity of the Ge crystals is enhanced by almost three orders of magnitude with respect to that of Ge epilayers directly grown on flat Si substrates. Electrical measurements performed on single heterojunction diodes formed between 3D Ge crystals and the Si substrate exhibit rectifying behavior with dark currents of the order of 1 mA/cm^2. For GaAs the thermal strain relaxation as a function of pattern size is similar to that found for group IV materials. Significant differences exist, however, in the evolution of crystal morphology with pattern size, which more and more tends to a pyramidal shape defined by stable {111} facets with decreasing width of the Si pillars.

1. Introduction

Attempts to extend Moore's Law [1] by introducing additional optical and electrical functionalities to the complementary metal-oxide-semiconductor (CMOS) platform, realization of high-efficiency solid state lighting, manufacturing of concentrator photovoltaic cells, and the fabrication of imaging detectors, especially for high-energy electromagnetic radiation, all require – in one form or another – the integration of crystalline materials with dissimilar lattice parameters on top of each other. Basically, this can be done either by a hybrid approach (e.g. various forms of wafer bonding and bump bonding techniques), or by heteroepitaxial growth.

In the case of hybrid technologies, reliability and costs are serious obstacles for their application on a large scale. That is because different thermal expansion coefficients induce mechanical stress, which may cause layer cracking and debonding of the wafers [2]. Moreover, for highly complex systems (e.g. imaging detectors), millions of separate components (e. g. pixels) have to be bump-bonded onto a wafer (e.g. CMOS processed read-out chip) [3].

When two dissimilar materials are combined by heteroepitaxial growth, mechanical stress may form as a result of different lattice parameters. When exceeding a certain thickness limit, this misfit stress is relieved either by elastic or plastic relaxation [4,5]. In the case of large misfit, initial stress relaxation usually occurs elastically by means of surface corrugation, for example in the form of islands [6]. For lower misfit, an epitaxial film may remain flat, while stress starts to be relieved plastically by misfit dislocations (MDs) at a certain critical film thickness

* Corresponding author at: OC Oerlikon Advanced Technologies, Iramali 18, FL-9496 Balzers, Liechtenstein. Tel.: +41 44 633 2261; fax: +41 44 633 1072.
E-mail addresses: cfalub@phys.ethz.ch, vkaenel@phys.ethz.ch (C.V. Falub).
[1] Present address: EMPA-Swiss Federal Laboratories for Materials Science and Technology, Lerchenfeldstrasse 5, CH-9014 St. Gallen.

0040-6090/$ – see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.tsf.2013.10.094

[7]. MDs are usually accompanied by threading dislocations (TDs) extending to the surface of the growing film [8]. Both MDs and TDs need to be spatially separated from the active region of a device, since they may degrade its performance to a large extent. While for finite misfit and sufficient layer thickness MDs always occur, threading dislocation densities (TDD) can be manipulated by various means.

There have been many approaches to lower TDD in blanket films [9–15]. While being partially successful, none of these methods resulted in a TDD below 10^6–10^7 cm^{-2} even for a simple system, such as Ge/Si(001) with a misfit of 4%.

It was realized long ago that a significant further reduction of TDDs can only be achieved by reducing the epitaxial growth area, i.e., by making the epitaxial structures small [16]. This can be done by depositing the epitaxial layers onto small substrate mesas (e.g. pillars) [17,18] or selectively into dielectric windows [19,20] previously defined by lithography and etching. The idea behind this is that with sufficient layer thickness, threading arms arising from the interface will exit the sides of the epitaxial structure, rather than reaching the upper surface. The concept was applied to various semiconductor combinations, such as Si, Ge, III–V and II–VI materials. It has become known under the name of "aspect ratio trapping (ART)" [20]. This method seems to work well for dielectric windows of submicron size, as long as neighboring epitaxial patches do not coalesce by lateral overgrowth of the mask. Once a continuous layer starts to form, however, dislocation densities again multiply by orders of magnitude. Moreover, upon coalescence and increasing film thickness, the problems of wafer bowing and layer cracking are bound to occur as a result of mismatched thermal expansion coefficients. The same may happen whenever a continuous film is cooled to room temperature after the epitaxial growth, seriously hampering subsequent processing steps, such as photolithography and patterning, or also further epitaxial growth [21]. These are serious problems when devices require layers with relatively large thicknesses, such as high-brightness light emitting diodes, multiple junction solar cells, or power transistors.

The problem of wafer bowing has been addressed in various ways in the past [22–24]. Unfortunately, however, reducing wafer bowing may even increase the tendency of layers to crack, because wafer bowing is associated with elastic stress relief.

Faced with the problem of realizing a low-cost, high-resolution and high-efficiency X-ray imaging detector consisting of a very thick Ge absorber layer monolithically integrated on a Si CMOS substrate, we have discovered a way suitable for solving thermal and lattice misfit problems at a stroke [25]. In order to efficiently absorb harder X-rays, the absorbing Ge layer should, however, be exceptionally thick (at least 50 μm), and have a low defect density to provide dark currents below 1 mA/cm^2 for a fully processed device. This challenging task became possible by replacing continuous semiconductor films tall, closely spaced crystals several microns in width. The method, coined "3D heteroepitaxy", rests on a combination of deep substrate patterning into tall pillars and self-limited lateral expansion during epitaxial growth. The method has been thoroughly tested for $Si_{1-x}Ge_x$ alloys grown on Si(001) substrate, for compositions ranging from pure Si to pure Ge [25].

Here, we show that 3D heteroepitaxy can be extended to other material combinations and substrate orientations, thus providing a conceptual platform for several device applications. By using scanning X-ray nano-diffraction and room temperature photoluminescence we show that it leads to strain-free, perfect crystals despite a heavily dislocated interface. The current–voltage (I–*V*) characteristics of heterojunction diodes formed by individual Ge crystals and the Si substrate exhibit rectifying diode behavior with sufficiently low dark currents (<1 mA/cm^2) for use in an X-ray detector.

2. Experimental details

Nominal 4″ (001)- and (111)-oriented (within ±0.5°), and 6° offcut Si substrates were patterned into arrays of uniformly spaced Si pillars and ridges by conventional photolithography and deep reactive ion etching (DRIE) based on the Bosch process [26,27]. Etch depths of 2 and 8 μm, pillar and ridge base widths ranging from 2 to 40 μm, and trench widths ranging from 1 to 5 μm were used in this work. Additionally, 100 μm thin 6″ CMOS wafers were patterned by the same procedure, with readout circuits located on the backside of the wafers. For electrical measurements and further device processing the patterned Si substrates were passivated by a ~90 nm thick SiO_2 layer apart from the top of the Si pillars.

Prior to epitaxial growth, the patterned Si substrates were cleaned using the standard RCA method. The native oxide was removed by a 5% hydrofluoric acid dip and subsequent rinse in ultrapure water. Once loaded into the growth chamber, the substrates were outgassed in ultra-high vacuum for 15 min at 300 °C before ramping to the growth temperature. Subsequently, pure Ge and $Si_{1-x}Ge_x$ alloy crystals were grown by low-energy plasma-enhanced chemical vapor deposition (LEPECVD) [28] at a rate of ~4 nm/s and temperatures ranging from 400 to 600 °C using germane (GeH_4) or silane (SiH_4) as reactive gases. The base and growth pressures in the chamber were around 1×10^{-9} mbar and ~2×10^{-2} mbar, respectively.

GaAs crystals were grown by metal–organic vapor phase epitaxy (MOVPE) onto 2 μm tall Ge crystals previously deposited on the patterned Si substrate by LEPECVD at 495 °C. We have used the standard method for the integration of III–V compounds on Si and bulk Ge substrates, usually referred to as the two-step growth method [29]. After a 7 nm thin, GaAs seed layer grown at 500 °C, GaAs crystals with heights ranging between 2 and 6 μm were grown onto the Ge/Si structures at 680 °C, a growth rate of ~0.5 nm/s and a pressure of ~100 mbar.

The morphology of the Ge, $Si_{1-x}Ge_x$ and GaAs crystals grown on the patterned Si substrates was monitored by Nomarski interference contrast optical microscopy (Nikon Eclipse 200D) and scanning electron microscopy (SEM) (Zeiss ULTRA 55 digital field emission). Crystal cross-sections were performed by means of a dual beam focused ion beam (FIB)/SEM, Zeiss NVision 40 with the Ga liquid metal ion source operated at 30 kV, imaging currents 10 pA, and milling currents up to 26 nA. The facet orientation was determined by atomic force microscopy (AFM) using a XE-100 microscope operated in non-contact mode, and transmission and scanning transmission electron microscopy (TEM, STEM) using a Tecnai F30ST TEM/STEM transmission electron microscope (FEI), operated at 300 kV. The specimens for TEM/STEM investigations were thinned to electron transparency by mechanical thinning followed by Ar-ion milling (4° incidence angle, 4 kV acceleration voltage). Defect etching was used to estimate the dislocation density. The Ge and SiGe crystals were etched for 40 s in a diluted iodine solution at 0 °C, and etch pits were counted by AFM.

High resolution X-ray diffraction (HRXRD) was used to investigate the crystalline quality and strain of the Ge crystals. Reciprocal space maps (RSMs) were recorded in the symmetric (004) and asymmetric (224) or (113) scattering geometries. As laboratory diffractometer we used a PANalytical X'Pert Pro-MRD (Cu $K\alpha_1$ radiation, beam diameter on the sample of ~1 mm) equipped with a 4-bounce Ge(220) crystal monochromator on the incident beam, as well as an analyzer crystal and a Xe point detector on the diffracted beam.

To assess the crystalline quality and tilt of individual crystals, scanning nano-diffraction experiments were performed at the ID01 beamline of the European Synchrotron Radiation Facility (ESRF) in Grenoble with a Huber diffractometer equipped with a high precision piezo (*x*,*y*,*z*) stage. The X-ray beam was focused down to ~300 × 500 nm by means of Fresnel zone plates. For a certain Bragg reflection, and a fixed (*x*,*y*) position, the incidence angle of the X-ray beam was scanned while moving the beam across the sample. Since a two-dimensional (2D) MAXIPIX pixel detector was used, 3D-RSMs were measured for each (*x*,*y*) position of the X-ray beam on the sample. The RSMs were recorded around symmetric (004) and asymmetric (115) reflections using a beam energy of 11.07 keV. 3D-RSMs were built from rocking scans, varying the incidence angle of the focused primary beam impinging the sample. Both