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Toward a tandem gallium phosphide on silicon solar cell through liquid phase epitaxy growth

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ABSTRACT

Three layers of GaP were epitaxially grown on Si(111) using liquid phase epitaxy (LPE) to demonstrate a path to fabrication of a GaP/Si tandem solar cell. Utilizing a Sn melt with Bi, Mg, and Si additives, direct epitaxial growth on a Si substrate occurred. This was followed by two further epitaxial growths, eliminating Si in the melt, with each layer decreasing in Si concentration. Scanning electron and optical microscopy and electron dispersive spectroscopy were performed in order to determine the characteristics of the growth layers. A fourth layer growth of GaP was attempted utilizing a Ga melt, and the existing structure was able to withstand contact with Ga without dissolution. Epitaxial layers of GaP with a decrease in Si concentration from 10-15% to 6%, then to less than 3%, were accomplished, thereby demonstrating a path to fabrication of a GaP/Si tandem cell using LPE.

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1. Introduction

One method to increase the energy conversion in solar cell devices is the tandem device structure. Presently, the materials used in the highest efficiency tandem structures are the III–Vs [1]. These materials, while providing high efficiencies, also are high cost. The goal of this work is to develop a methodology for combining the high efficiency of III–V tandem structures with the low cost of silicon substrates.

GaP, with a bandgap of 2.26 eV and a lattice mismatch with Si of 0.37%, holds promise for the growth of III–V on Si devices using liquid phase epitaxy (LPE). The bandgap of GaP is too high, however, to be the optimum material for the top cell in a III–V/Si tandem [2]. The ideal top cell bandgap in a III–V/Si tandem is lower than that of GaP, so using the GaP growth as a nucleation layer rather than an active device allows the III–V top cell to collect the higher energy photons with GaP remaining transparent to any photons passing to the Si device. From a material growth perspective, GaP provides a good foundation for further III–V growth [3–5]. GaP could be alloyed with, for example, In to achieve a more optimal bandgap without sacrificing lattice matching. The bandgap of $Ga_xIn_{1-x}P$ could be varied as needed by changing the stoichiometry. GaP on Si, therefore, provides both high-quality growth and a foundation for the growth of other III–V materials to extend the value of the device.

Previously, Huang [6] demonstrated high-quality crystalline growth on Si(111), both with a perfectly aligned and a 4° miscut substrate. The resulting epitaxial layers had a Si concentration of 15–20%. Si is a known dopant of GaP, but evidence of large inclusions of Si were found. Additionally, there is unintentional doping of the GaP layer by Sn — producing a strong n-type layer on the order of 10^{17} cm^{-3} [7]. This resulting layer is not suitable for the active layer of a device. The Si introduces defects in the crystal, and growth of a p-type layer requires compensation doping that would further reduce any device performance. The advantage of this layer is its ability to quickly grow a GaP buffer layer directly on a Si substrate.

Another LPE technique for the growth of epitaxial GaP is from Lu [8,9], which has been used to grow a GaP solar cell on a GaP substrate from a Ga melt. While this methodology produces well-performing GaP solar cells, Ga cannot be used as the solvent for growth of GaP on Si because of the high solubility of Si in Ga.

This work presents improvements to the previous growth method for GaP on Si, as well as demonstrates the direction for future improvement and device growth utilizing the method for growing GaP on GaP.

2. Experimental

The LPE system used for this research was a three zone sliding horizontal furnace which surrounded a quartz tube holding the samples in a purified hydrogen-rich environment. The substrates and melts were

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held in a graphite boat with a horizontal slide bar. The slide bar was manually controlled through the movement of a quartz rod. A schematic of the furnace is shown in Fig. 1.

Si substrates were prepared for loading into the system following standard Si cleaning procedures [10,11]. An RCA1 clean was performed for 15 min, followed by a dip into a 1% HF solution just long enough for the samples to become hydrophobic. The samples were then cleaned in RCA2 for 10 min, briefly immersed in 1% HF, and loaded into the furnace. For substrates that already had a layer of GaP grown, an acetone, methanol, then isopropanol rinse replaced the RCA1. The RCA2 procedure for substrates with GaP present had a reduced cleaning time of 3 min.

After loading the samples and melt components, the system was sealed and pumped to 6.67 Pa or lower, purged with Ar, for three total pump and purge segments. The atmosphere was then switched to purified H_2.

Initial determinations of growth results were performed using an optical microscope. Following visual confirmation of the existence of growth layers, the samples were analyzed using a JEOL JSM-7400F SEM with an Oxford INCA EDS system for characterizing growth morphology and composition. GaP growth layers were then observed using a Zygo NewView 700s to determine growth thickness from a three dimensional optical surface profile.

The growth of GaP on Si from a Sn melt was based on previous work by Huang [6], which demonstrated high-quality crystalline growths on Si(111), both with an aligned and a 4° miscut substrate. Films grown on perfectly aligned substrates had thicknesses of 200 nm and displayed circular plateaus of growth, indicating fault lines possibly due to anti-phase domain (APD) development. In addition, threading dislocation density (TDD) was measured at 10^6 cm^{-2}, and a 26–68% Si concentration for plateaus and planar regions, respectively. Films on miscut substrates were 800 nm thick, displayed uniform grains across the film, a TDD of 10^8 cm^{-2}, and uniform 15% Si concentration throughout.

Melt composition from Huang's work included 3.5 g of Sn as the solvent, 350 mg of Bi for substrate wetting, 2–3 mg of Mg for native oxide removal, and 75 mg GaP powder as the source for growth. Si was introduced into the melt using a source wafer. The standard time–temperature profile, as shown in Fig. 2, began with a ramp from ambient temperature to 910 °C over a period of 60 min. Melt saturation occurred at 910 °C for 60 min to dissolve the GaP in the Sn. The temperature was then reduced to 750 °C in 60 min, and held for 65 min, with

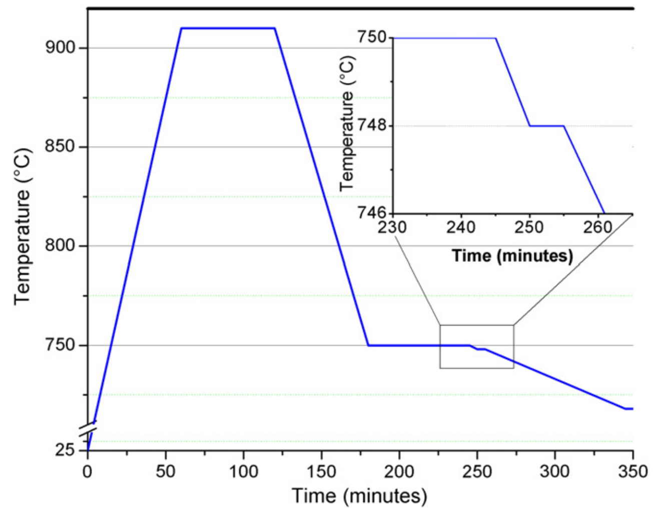

Fig. 2. Standard time temperature profile, showing initial ramp and GaP homogenization, ramp down and Si saturation, supersaturation, and growth.

the melt held over the Si source wafer for the final 35 min. Finally, growth began by transferring the melt to the seed wafer after a 2 °C supersaturation at a cooling rate of 1 °C per 3 min. The procedure just described, as developed by Huang, will be referred to as the standard procedure, and any deviations from the standard will be noted where applicable.

3. Results & discussion

The goal for GaP-based device growth using LPE is to transition from the present Sn melt for the buffer layers to a Ga melt for the device layers, the latter of which is described by Lu et al. [9]. Attempts to grow from a Ga melt on the standard GaP on Si sample resulted in the sample being completely dissolved by the Ga melt — indicating that further measures must be taken to 1) reduce the concentration of Si in the epitaxial layer and 2) protect the Si substrate from contact with the Ga. The presence of 15% Si in the GaP layer is too high a concentration for Si to be acting purely as a dopant. Si in the Sn melt is explained by

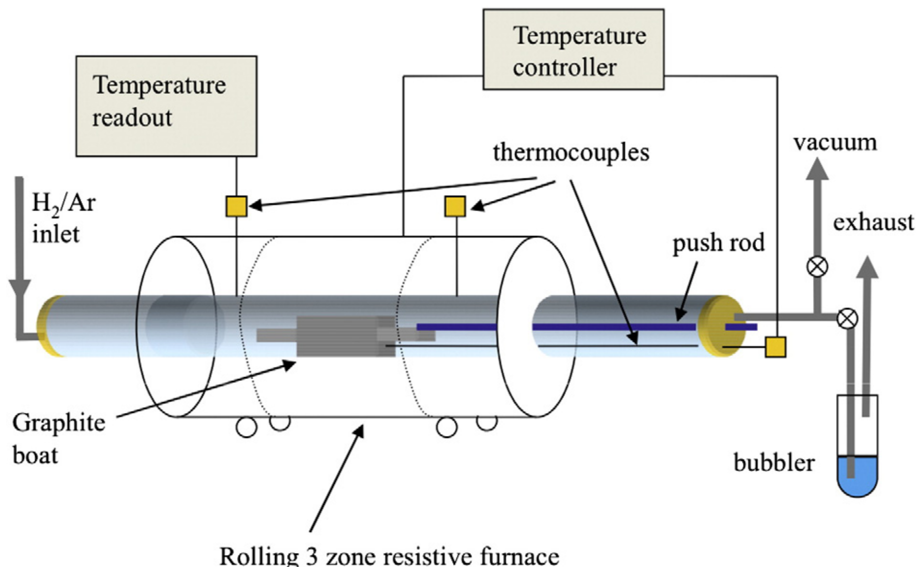

Fig. 1. A schematic of the LPE system used in this work [6].

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