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Low-temperature fabrication of Y_2O_3/Ge gate stacks with ultrathin GeO_x interlayer and low interface states density characterized by a reliable deep-level transient spectroscopy method

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ABSTRACT

Y_2O_3/Ge gate stacks with ultrathin GeO_x interlayer were fabricated by two-step rf sputtering using a Y_2O_3 target followed by a vacuum-annealing, which were carried out in the same chamber without vacuum breaking. TiN-gate Ge metal–insulator–semiconductor (MIS) capacitors were fabricated with equivalent oxide thicknesses in the range of 2.1–2.3 nm. The highest temperature was 400 °C for the entire fabrication process. Interface states density (D_{it}) was characterized using a deep-level transient spectroscopy method with optimized injection pulse and quiescent reverse-bias voltages at each temperature. D_{it} values were approximately 4×10^{13}, 5×10^{11}, and 3×10^{12} cm^{-2} eV^{-1} at energy positions around valence band, mid-gap, and conduction band, respectively. The slow trap contribution was also small in the upper half of the band-gap, implying a potential application of the Y_2O_3/Ge gate stack to the fabrication of high-performance Ge-n-MIS field effect transistors.

1. Introduction

The next generation of ultra large scale integration requires channel materials with carrier mobility superior to that of Si. For this purpose, owing to high carrier mobility of Ge, Ge metal–insulator–semiconductor field effect transistors (MISFETs) are being comprehensively studied [1–3]. To fabricate a high-performance Ge-MISFET, essential issues should be considered such as the fabrication of high-quality source/drain (S/D) and the reduction of interface-state density (D_{it}). In particular, it has been found that Ge-n-MISFET shows poor performance that caused by poor quality of S/D n^+–p junction formed by ion implantation, due to a low solubility and a large diffusion constant of n-type dopants in Ge [4,5]. To improve the quality of Ge n^+–p junction, instead of ion implantation, thermal diffusion methods such as gas-phase doping of As [6] and solid source diffusion of Sb [7] have been performed. However, the low dopant solubility is still an issue.

Besides a p–n junction, a Schottky contact is also a practical way for fabricating high quality S/D. Recently we have fabricated TiN/Ge contact with extremely low electron barrier height of 0.09 eV [8] at room temperature, implying practical application to high-performance Schottky S/D Ge-n-MISFET fabrication [9]. However, it has been found that the TiN/Ge contact must be fabricated at temperatures not more than 400 °C, otherwise the electron barrier height would drastically increase with increasing temperature [10].

To fabricate a high-performance Ge-MISFET, high-k gate stacks with low D_{it} are always desired. Since a GeO_2/Ge structure exhibits good interfacial property [11,12], GeO_2 and GeO_x interlayers (ILs) have been widely studied for improving performance of Ge MISFETs [1–3,6]. However, since the lateral etching of GeO_x is a serious issue for a gate-first process, a gate-last process is preferred to employ GeO_x IL in a Ge MISFET fabrication. Considering the low temperature of TiN/Ge fabrication process, a low temperature gate fabrication process has to be developed for Ge-n-MISFETs with the TiN/Ge Schottky S/D. In general, to improve interface property, relatively high temperature (550 °C) is employed for Ge oxidation [2] or post-deposition annealing (PDA) [3]. Therefore, it is a challenge to fabricate a high-k gate stack with a GeO_2 IL and a low D_{it} by using a low-temperature process. Furthermore, small equivalent oxide thickness (EOT) is also essential for realizing advanced Ge-MISFETs, which requires a small thickness of GeO_2 IL.

Recently, Al_2O_3/GeO_x/Ge gate stacks with ultrathin GeO_x IL and a low D_{it} have been fabricated by electron cyclotron resonance plasma post-oxidation with a maximum processing temperature of 400 °C [13], implying that a plasma oxidation is more suitable than thermal oxidation for low temperature fabrication of high-quality high-k gate stacks on Ge.

Considering interface property, Y_2O_3 is also a good candidate for high-k gate stack fabrication on Ge. It has been found that Y_2O_3 can improve GeO_2/Ge interface properties by so-called valency passivation that Y may work as a self-compensation site of a small number of dangling bonds or oxygen-deficient sites in GeO_2 [14]. However, the GeO_x IL was fabricated by a thermal oxidation at 550 °C for the reported Y_2O_3/GeO_x/Ge gate stacks [2], which exceeded the temperature

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limitation of 400 °C as mentioned above. To solve this problem, a non-thermal-equilibrium process should be used for GeO_x IL formation.

In this paper, we demonstrated a low-temperature fabrication of Y_2O_3/Ge gate stacks with ultrathin GeO_x IL and low D_{it}, which was performed by a simple process of two-step rf sputtering using a Y_2O_3 target followed by a vacuum-annealing at 400 °C in the same chamber without vacuum breaking. D_{it} was characterized by an accurate deep-level transient spectroscopy (DLTS) method using optimized injection pulse and quiescent reverse-bias voltages (V_P and V_R, respectively) at each fixed temperature [15].

2. Experimental details

Both n- and p-type (100) Ge substrates with respective resistivity of 0.29 and 0.38 Ωcm were used. Fig. 1 shows the fabrication process of Y_2O_3/Ge gate stacks. After the surface was cleaned with acetone and then repeatedly dipped in 10% hydrofluoric acid and rinsed in deionized water, sacrificial oxidation was performed at 450 °C for 30 min by dry oxidation. Then the substrates were set into a physical vapor deposition (PVD) chamber with a base pressure of less than 3×10^{-5} Pa. To form a GeO_x IL with good interface property, it is very important to complete the fabrication process of high-k gate stacks without breaking the vacuum [16].

After a surface cleaning done through GeO_2 volatilization by a step-mode vacuum-annealing [16], three essential processes were performed in the same PVD chamber, as shown in Figs. 1(a), 1(b), and 1(c). First, a radio frequency (rf) sputtering was performed using a Y_2O_3 target and an rf power (P_{rf}) of 5 W at room temperature (RT) for 10 min with the addition of O_2 in gas ambience. The gas pressure was kept at 1.0 Pa with Ar and O_2 flow rates of 20 and 0.2 sccm, respectively. In this step, even though a Y_2O_3 target was used, GeO_x IL was formed due to the low P_{rf}, which will be discussed later. Then, a 3 nm-thick Y_2O_3 layer was deposited at RT by rf sputtering without O_2 addition in the gas ambience, for which the gas pressure was kept at 1.0 Pa with a Ar flow rate of 20 sccm, and the P_{rf} was 20 W. After that, a PDA was carried out at 400 °C for 30 min in vacuum with a pressure of 7.5×10^{-5} Pa.

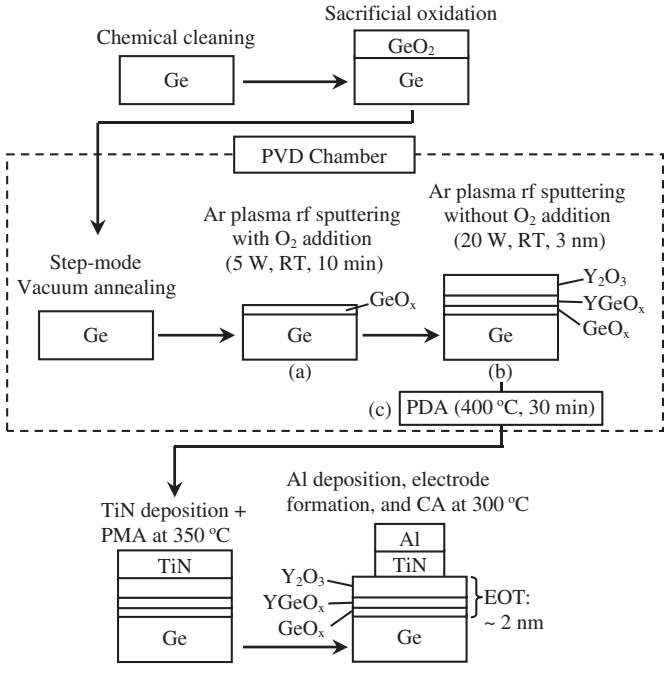

Fig. 1. Fabrication process of Ge-MISCAPs with $Y_2O_3/YGeO_x/GeO_x$/Ge gate stacks. PVD, rf, RT, PDA, PMA, and CA are defined in the text.

Then the sample was taken out of the PVD chamber for a 50 nm-thick TiN deposition using Ar plasma rf sputtering at RT with a gas pressure of 2.0 Pa, a Ar flow rate of 30 sccm, and a P_{rf} of 60 W. A post-metallization annealing (PMA) was also performed at 350 °C for 20 min in N_2 ambient. Finally, a 100-nm-thick Al film was deposited by thermal evaporation followed by gate patterning [17] and a contact annealing (CA) carried out at 350 °C for 10 min in N_2 for obtaining electrically good adhesion between Al and TiN films.

To clarify the components of important layers of the gate-stacks, after each essential fabrication step, X-ray photoelectron spectroscopy (XPS) measurements were performed using AXIS 165 (SHIMADZU KRATOS ANALYTICAL LTD.) with Al Kα line of 1486.49 eV (high voltage: 15 kV; emission current: 7 mA; diameter of measured area: 1 mm) at a photoelectron take-off angle of 90°, and calibrated using a Ge 3d core level (29.3 eV). For all the Ge metal–insulator–semiconductor capacitors (MISCAPs), capacitance–gate bias voltage (C–V_G) characteristics were measured using an Agilent 4294A impedance analyzer at 1 MHz. D_{it} was evaluated by DLTS measurements using a SEMILAB DLS83D system with a lock-in integrator.

3. Results and discussion

To fabricate high-performance Ge-MISCAPs with high-k gate stacks, the essential issue is to form an IL with good interface property. Since the temperature was limited to be no more than 400 °C, instead of a thermal oxidation process, an Ar plasma rf sputtering process was used to form GeO_x IL on Ge, as shown in Fig. 1(a), of which the XP spectrum is shown in Fig. 2(a). Ge 3d spectra were clearly observed at a binding energy of 32.9 eV, which is close to GeO_2 peak, implying a GeO_x layer formation with atomic fractions similar to that of GeO_2. Although an Y_2O_3 target was used, no Y 4p signal was observed, implying that the Y_2O_3 deposition could hardly occur under the low P_{rf} of 5 W. Even though very few Y atoms might exist in the GeO_x layer, they are negligible by comparing with the Y atoms diffused into GeO_x IL in the following steps. Note the GeO_x layer was formed at RT, which is the advantage of plasma oxidation. By using a spectroscopic ellipsometer, a physical thickness of approximately 3 nm was measured for the GeO_x layer.

An Y_2O_3 layer was deposited as a high-k dielectric film by the process of Fig. 1(b), of which the XP spectrum is shown in Fig. 2(b). A Y 4p peak was clearly observed, implying the deposition of Y_2O_3 layer. Simultaneously, the GeO_x peak intensity significantly decreased and a

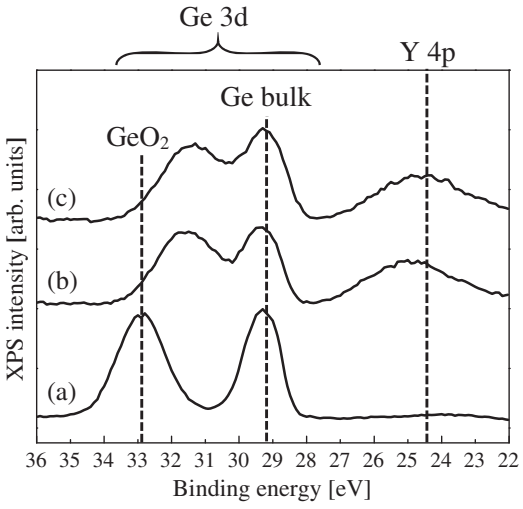

Fig. 2. XP spectra of samples (a) just after rf sputtering with O_2 addition and a P_{rf} = 5 W, (b) after 3 nm-Y_2O_3 deposition by rf sputtering without O_2 addition and with a P_{rf} = 20 W, and (c) after 400 °C PDA.