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Radiation tolerance of $Si_{1-y}C_y$ source/drain n-type metal oxide semiconductor field effect transistors with different carbon concentrations

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ABSTRACT

The 2-MeV electron radiation damage of silicon–carbon source/drain (S/D) n-type metal oxide semiconductor field effect transistors with different carbon (C) concentrations is studied. Before irradiation, an enhancement of the electron mobility with C concentration of the S/D stressors is clearly observed. On the other hand, after electron irradiation, both the threshold voltage shift and the maximum electron mobility degradation are independent on the C concentration for all electron fluences studied. These results indicate that the strain induced electron mobility enhancement due to the C doping is retained after irradiation in the studied devices.

1. Introduction

The scaling of complementary metal oxide semiconductor technologies leads to an intrinsic hardening against certain radiation effects, so that the development of ultra-large-scale integration components and circuits for harsh environments is becoming more popular [1]. This has been driven by multiple factors, including the implementation of microelectronics components and circuits in nuclear plants, high-energy particle accelerators and artificial satellites. On the other hand, in terms of high mobility substrates, channel materials and methods for creating strained channels are being explored [2–4]. The potential of local compressive strain, based on the embedded or recessed silicon–germanium ($Si_{1-x}Ge_x$) source/drain (S/D) method in p-type metal oxide semiconductor field effect transistors (p-MOSFETs) has been demonstrated in the 22 nm node and beyond [5]. For n-type MOSFETs (n-MOSFETs), the electron mobility and drive current are enhanced by the tensile strain in the Si channel caused by the difference in the lattice constant between the Si channel region and the embedded silicon–carbon ($Si_{1-y}C_y$) S/D stressors [6,7]. However, the reliability of locally strained MOSFETs in a radiation harsh environment is not well investigated. In order to resolve this issue, we have recently studied the degradation of the device performance with 2-MeV electron irradiation in regard to the $Si_{1-x}Ge_x$ S/D p-MOSFETs [8]. It had been shown that the hole mobility enhancement effect by strained Si channel has been retained after 1×10^{17} e/cm^2 electron irradiation [8]. In the present paper, we investigate the electrical degradation of $Si_{1-y}C_y$ S/D n-MOSFETs irradiated by 2-MeV electrons.

2. Experimental procedure

2.1. Sample preparation

Fig. 1 shows a schematic cross-sectional view of the $Si_{1-y}C_y$ ($y = 0$, 0.01, 0.015) S/D n-MOSFETs fabricated on 200 mm p-type silicon wafers at imec. Active diode regions are defined by shallow trench isolation, followed by boron p-well implantations. Extension and halo implantations were also performed. Subsequently, a highly-doped drain implantation of 4 keV phosphorus ions at a dose of 5×10^{15} cm^{-2} was carried out. The trenches of the S/D regions were dry-etched to a depth of 90 nm and were refilled with in-situ highly phosphorus doped $Si_{1-y}C_y$ epitaxial layers with carbon concentrations $y = 0.01$ and 0.015, using an Epsilon® chemical vapor deposition tool manufactured

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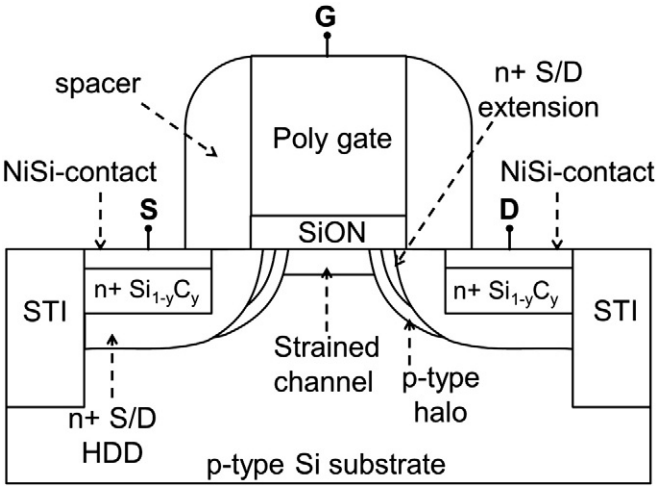

Fig. 1. Schematic cross-sectional view of the $Si_{1-y}C_y$ S/D n-MOSFETs.

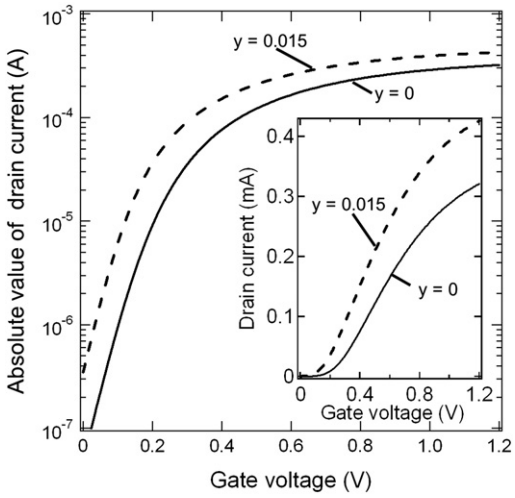

Fig. 2. Input characteristics of $Si_{1-y}C_y$ S/D n-MOSFETs before electron irradiation.

by ASM International NV. Unstressed reference Si transistors were also processed in order to allow comparison. Dopant activation was achieved by a 950 °C spike annealing. The studied transistors were fabricated with a 1.5 nm SiON/poly-Si gate stack, 10 μm gate width and 0.25 μm gate length.

2.2. Experimental conditions

These devices were irradiated with 2-MeV electrons at fluences of 1×10^{16} and 1×10^{17} e/cm^2 at room temperature without applied bias. The electron accelerator at Takasaki Japan Atomic Energy Agency was used for the irradiations. The fluence rate was fixed at 4.68×10^{13} e/(cm^2·s). The degradation of the device performance of $Si_{1-y}C_y$ S/D n-MOSFETs was evaluated using the input (I_{DS}–V_{GS}) characteristics at a drain voltage (V_{DS}) of 0.025 V and gate voltages (V_{GS}) ranging from 0 to 1.2 V. The threshold voltage (V_{TH}) was extracted from linear extrapolation of the input characteristics. In addition, the electron mobility (μ_n) was calculated using to Eq. (1), where L, W, and C_{OX} represent gate length, gate width, and capacitance of gate oxide, respectively.

$$\mu_n = \frac{\partial I_{DS}}{\partial V_{GS}} \cdot \frac{L}{W \cdot C_{OX}} \cdot \frac{1}{V_{DS}} \quad (1)$$

3. Results and discussions

First, the effect of the tensile strain in the Si-channel of $Si_{1-y}C_y$ S/D n-MOSFETs induced by different C concentrations was evaluated. Fig. 2 shows the input characteristics of $Si_{0.985}C_{0.015}$ S/D n-MOSFETs ($y = 0.015$) and a reference Si-MOSFET ($y = 0$) before electron irradiation. Before electron irradiation, from the linear axis I_{DS}–V_{GS} figure in the inset, the gradient of the drain current at a gate voltage from 0.4 to 1.2 V increases with C doping. At the same time, from logarithmic axis I_{DS}–V_{GS} figure, the subthreshold current exhibits a negative shift at a gate voltage from 0 to 0.4 V in the case of $Si_{0.985}C_{0.015}$ S/D n-MOSFETs. Fig. 3(a) and (b) shows the maximum μ_n and the V_{TH} of $Si_{1-y}C_y$ S/D n-MOSFET, as a function of C concentration ($y = 0$, 0.01 and 0.015), respectively. According to Vegard's law, the $Si_{1-y}C_y$ alloy has a smaller lattice constant (a_{SiC}) than the lattice constant (a_{Si}) of Si. The a_{SiC} is given by Eq. (2),

$$a_{SiC} = (1-y) \cdot a_{Si} + y \cdot a_C \quad (2)$$

where $a_{Si} = 0.543$ nm and $a_C = 0.356$ nm. In addition, the strain ratio of the $y = 0.01$ and 0.015 samples is given by Eq. (3), and they have approximately 0.35% and 0.52% tensile strain, respectively.

$$\text{Strain ratio} = a_{SiC}/a_{Si}. \quad (3)$$

In Fig. 3(a), the μ_n enhancement in the tensile strained Si channel, due to the $Si_{1-y}C_y$ S/D stressors is clearly shown. This μ_n enhancement gives rise to the drain current increase with increasing C concentration. By contrast, in Fig. 3(b), the V_{TH} exhibits a limited tensile strain induced V_{TH} change with C concentration. This result, in line with literature observations [9], suggests that a tensile strain induced band gap shrinkage; it is the cause of the negative shift of the subthreshold current. Therefore, the variation of the drain current with C concentration could be mainly attributed to the presence of tensile strain in the Si-channel.

Next, the effect of electron irradiation on the electrical performance of n-MOSFETs fabricated with tensile strained Si channels is discussed. Fig. 4 shows the input characteristics of 2-MeV electron irradiated $Si_{0.985}C_{0.015}$ S/D n-MOSFETs. After 2-MeV electron irradiation, the subthreshold current at a gate voltage from 0 to 0.4 V did not remarkably change for the studied electron fluences. However, the drain current at a gate voltage 0.4 to 1.2 V decreases by electron irradiation. When the MOSFETs are irradiated with 2-MeV electrons, electron–hole pairs are generated in the gate oxide by ionization. Simultaneously, the lattice defects are generated in the Si bulk region because atoms are moved out from substitutional lattice sites to interstitial lattice sites. Generation of

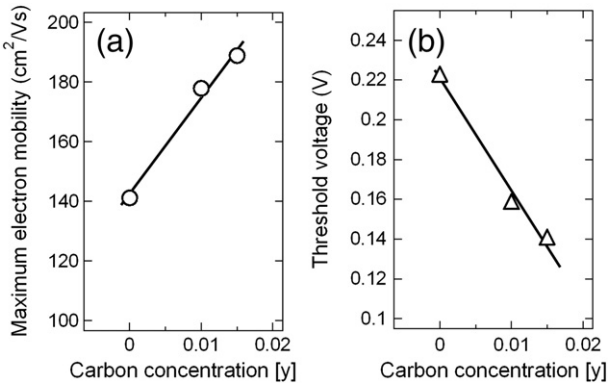

Fig. 3. Maximum electron mobility (a) and threshold voltage (b) and of $Si_{1-y}C_y$ S/D n-MOSFETs before electron irradiation.