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Effects of extended poly gate on the performance of strained P-type metal-oxide-semiconductor field-effect transistors with a narrow channel width

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ABSTRACT

The layout patterns of nano-scale devices have significant impacts on device performance when an increase in operating velocity is considered. Thus, advanced strain engineering of metal-oxide-semiconductor field-effect transistors (MOSFETs) is necessary when highly scaled gate lengths are employed. The foregoing mechanical effects are observable when a device with a narrow channel width is utilized. However, when a device integrated with an extended poly gate is scaled down to several hundreds of nanometers, the induced stress contours of the channel region and corresponding mobility gain become troublesome and must be resolved.
This study investigates the mechanical impacts of extended gate widths on the mobility gains of p-type MOSFETs. The selected MOSFET has a SiGe stressor embedded in its source and drain regions, as well as a compressive contact etch stop layer. Three-dimensional finite element simulation is performed to emulate the stress contour within the Si channel and estimate the related mobility gain. Sensitivity analyses of the simulation results using factorial designs and response surface methodology indicate that stresses within the Si channel are induced by a bending force determined by the extension of the poly width. A significant enhancement in mobility gain is found when an extended poly width combined with proper arrangements of the device geometry is applied.
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1. Introduction

Strain engineering is an important means of enhancing the performance of advanced metal-oxide-semiconductor field-effect transistor (MOSFET) devices when scaling down of electronic transistors is required [1–4]. Addition of intentional stresses on the source and drain (S/D) regions of p-type MOSFET (PMOSFET) transistors combined with a compressive contact etch stop layer (CESL, a strained-Si nitride cap layer) is regarded as an effective method by which mobility gains may be significantly increased. The mobility gain in device channels is directly enhanced by lattice mismatch stresses generated by SiGe alloys embedded in the S/D region [5]. SiGe lattices obtained under different Ge mole fractions are calculated using Vegard's law. Several studies have explored the influences of factors including SiGe thickness, Ge concentration, and the space between the Si channel and the S/D region on the induced strain within a device channel [6]. When the SiH:N:He gas ratio and process pressure are controlled, for example, the CESL can bear different stress magnitudes. From the viewpoint of manufacturing processes, plasma-enhanced chemical vapor deposition (CVD) and low-pressure CVD may be used to achieve CESLs bearing either a compressive or tensile stress [7]. In CESLs, the gate height is a dominant factor that determines the stress distribution of Si channels [8]. An increase in stress has been observed to result in shortening of the poly height. Moreover, stress signatures along the direction of the channel length under a loaded CESL exhibit reversal as a large extent of gate length is examined [9].

Information on the mechanical impacts of extended poly gates is limited since most published studies have focused on regular devices. As transistors are continuously scaled, the effects of extended poly gates on stress distributions in the channel region must be analyzed. Although several studies have established the effects of the channel width on stress contours within relevant devices [4,10], technical reports on the mechanical load exerted on a narrow MOSFET channel width resulting from an extended poly gate width are scarce (Fig. 1).

Critical issues on overall layout designs must be resolved because extended poly gates are often utilized in actual devices. The present study uses a three-dimensional (3D) finite element process-oriented simulation employing factorial designs to explore the stress distribution in a PMOSFET under various geometrical device structure combinations with an extended poly width layout pattern (Fig. 1). The PMOSFET selected for stress/strain emulated analyses has an embedded SiGe stressor in its S/D region and a compressive CESL. The simulations focus on the effects of specific factors, such as S/D SiGe alloy and CESL stressors, on device performance. In this work, the stress induced by shallow trench isolation (STI) is considered minor compared with the

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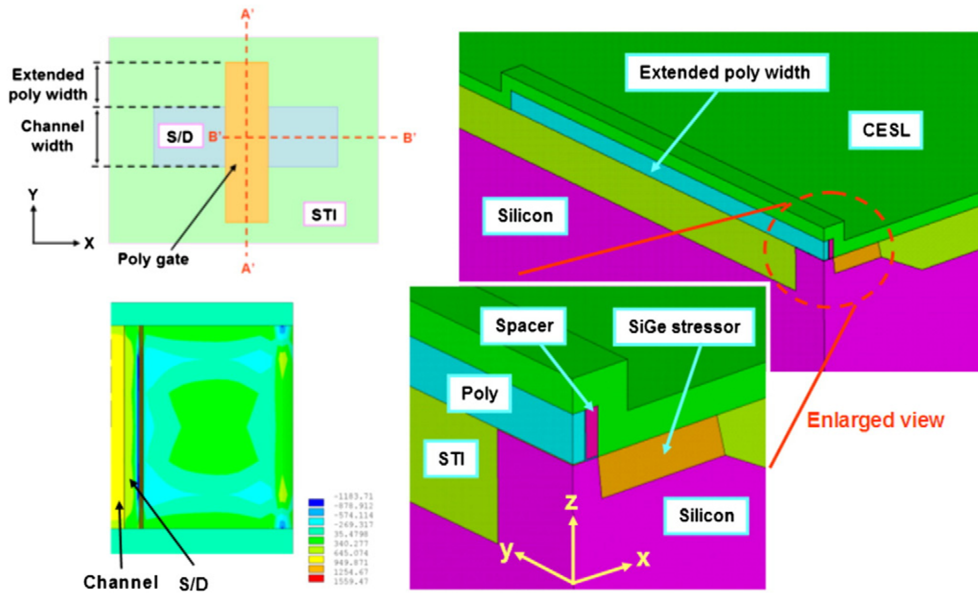

Fig. 1. Schematic of the PMOS device structure used in the simulations. Here, x represents the [110] plane, y denotes the [−110] plane, and z represents the [001] plane.

stresses contributed by S/D SiGe and CESL stressors [11,12]. As such, the stress effects of STI on the numerical simulations are ignored in this study. Interactions between two major design factors are systematically analyzed by means of central composite design (CCD) to determine the extent by which these factors influence the mobility gain of the resultant devices.

2. Device stress estimations and experimental designs

2.1. Stress simulation

Fig. 1 (top left) shows the layout used for the 3D stress process-oriented simulation, which was carried out by ANSYS® software. A biaxial symmetry was assumed for the PMOSFET device structure, which was surrounded by STI. One quarter of the finite element model was constructed to reduce the number of elements and nodes involved and increase the efficiency of computer calculations. Each component in the stress simulation is labeled (Fig. 1, right side).

The length and height of the poly gate were 40 and 60 nm, respectively, and the CESL thickness was 50 nm. A device with a narrow channel width is evidently affected when it is subjected to various bending behaviors by changing the extended poly width. Under the boundary conditions induced by displacement constraints in the corresponding symmetry planes, intrinsic stresses of −2.0 GPa for the CESL and 25% Ge for the SiGe alloy were separately applied in the stress simulations to determine the resultant effects of induced stress on the Si channel region. The left bottom image in Fig. 1 shows one instance of the stress contour along the width direction under a 40 nm gate length and 3 μm gate width. Fig. 2 shows the simulation methodology adopted in this study. To examine variations in mobility gain as a function of the length of the extended poly gate, 3D analysis was performed. The induced lattice mismatch stress presented by the SiGe alloy and the intrinsic stress presented by the CESL were managed using the coefficient of thermal extension approach; this approach is a calculated mechanics-based method and not a built-in function of the simulation software [13]. The process-flow simulation technique utilized in this investigation effectively shows the true stress contours of MOSFET devices when the mechanical behavior of step-by-step stress relaxation during film deposition is taken into account [14]. Using the electrical data presented in our previous study, the proposed simulation approach and predicted results were verified to be highly reliable [15]. The two-dimensional (2D) and 3D analytical results (width dependence stress estimations of the tested PMOSFET) obtained using the proposed simulation approach were consistent with the findings by Wang [16].

2.2. Mobility estimation

MOSFET mobility enhancements attributed to mechanical stress components can be approximated using the classical piezoresistance mobility model shown in Table 1. The vertical stress in PMOSFETs has a negligible effect on device performance because of low piezoresistance coefficient along this direction [17]. As such, only the biaxial stress components were considered in this investigation. Because reliable testing data on the piezoresistive coefficients in the inversion layers were not derived, bulk values were approximated. The use of bulk piezoresistive coefficients was validated as a beneficial equivalence through wafer bending measurements [18]. Thus, the piezoresistive coefficients of bulk Si (Table 1) employed in this study are highly reliable.

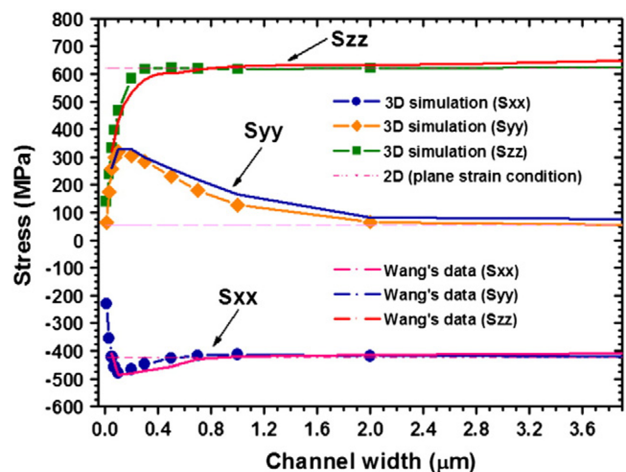

Fig. 2. Predicted results validated with the presented simulation methodology and Wang's data[11] on the channel width dependence of stress components (S_{xx}, S_{yy}, and S_{zz}) within the Si channel region for PMOSFET with a 40 nm gate length and S/D SiGe alloy stressors at 25% Ge mole fraction.

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