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Atomic layer deposition of dielectrics for carbon-based electronics

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ABSTRACT

Carbon based nanomaterials like nanotubes and graphene have emerged as future generation electronic materials for device applications because of their interesting properties such as high-mobility and ability to carry high-current densities compared to conventional semiconductor materials like silicon. Therefore, there is a need to develop techniques to integrate robust gate dielectrics with high-quality interfaces for these materials in order to attain maximum performance. To date, a variety of methods including physical vapor deposition, atomic layer deposition (ALD), physical assembly among others have been employed in order to integrate dielectrics for carbon nanotube and graphene based field-effect transistors. Owing to the difficulty in wetting pristine surfaces of nanotubes and graphene, most of the ALD methods require a seeding technique involving non-covalent functionalization of their surfaces in order to nucleate dielectric growth while maintaining their intrinsic properties. A comprehensive review regarding the various dielectric integration schemes for emerging devices and their limitations with respect to ALD based methods along with a future outlook is provided.

1. Introduction

Semiconductor industry has been driven on the principle of Moore's law which predicted that increasing the density of basic components (such as metal-oxide-semiconductor field-effect transistors — MOSFETs) of an integrated circuit (IC) would result in increased performance, functionality and decreased costs [1]. This has been achieved by scaling the transistor size following the MOSFET scaling rules outlined by Dennard et al. [2]. Silicon has been the most widely used material to-date in ICs for the majority of applications. The continuous scaling of transistor size required introduction of several material and structural changes to the silicon complementary metal-oxide-semiconductor (CMOS) technology. Some of the major changes include — (1) introduction of epitaxial SiGe for source/drain regions (starting at the 90 nm node) for inducing strain in the channel in order to obtain increased carrier mobilities [3], (2) replacement of conventional silica (SiO_2)/poly-Si gate stack with higher dielectric constant (high-κ) materials such as hafnium-zirconate and metal gate (starting at the 45 nm node) to avoid unacceptably high gate leakage currents and to eliminate additional parasitic capacitance [3], (3) introduction of Multi-gate/Tri-gate structures (starting at the 22 nm node) to have better electrostatic control of the channel [4]. With further materials and process innovations, International Technology Roadmap for Semiconductors (ITRS) 2011 predicts that silicon based CMOS technology could be extended ("More Moore") up to year 2018, beyond which alternative channel materials and device architectures will need to be introduced into ICs in order to have enhanced performance [5]. There are a variety of materials which are currently under investigation and some of the most promising materials included in ITRS 2011 are bulk Si like materials such as III–V compounds (InGaAs, GaSb) and Ge, layered 2D materials like Graphene and one-dimensional materials like carbon nanotubes (CNTs).

The semiconductor industry is also searching for more functionality in a chip ("More than Moore"). In order to effectively provide more functionality, such as analog and radio frequency (RF) devices and power devices, etc., it is frequently recommended to use alternative channel materials to have enhanced properties, such as, higher carrier mobility, break-down voltages, etc., compared to conventional Si. As wireless communication technology is playing a key role in various human activities in modern society, the demand for high performance RF devices has increased. RF transistor performance is frequently characterized by the cut-off frequency, ($f_T = g_m/2\pi C_g$; g_m is the transconductance and C_g is the gate capacitance) representing how fast the current in a channel can be modulated by a gate. Since, g_m is directly proportional to the carrier mobility in the channel, carbon based nanomaterials such as CNTs and graphene, as well as compound semiconductors are expected to be good candidates for RF switches because of their high carrier mobilities. The intrinsic f_T of graphene based field-effect transistors (FETs) with gate length of 50 nm or less is expected to be higher than 1 THz [6,7]. As in the case of MOSFETs, scaling down the equivalent oxide thickness (EOT) of gate dielectrics is also important, not only for enhancement of g_m, but also for f_T performance against parasitic capacitances [8].

Since the possibility of a ballistic THz nanotube transistor was predicted [9] and a CNT transistor operation at 2.6 GHz was experimentally

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demonstrated [10], high frequency performance of a CNT transistor has attracted a lot of attention [11,12]. However, its performance does not reach to one tenth of the expected intrinsic f_T due to various practical integration issues, including density, alignment and contact of CNT as well as metallic CNT impurities, etc. A semiconducting CNT is expected to have a bandgap with a relatively low mobility compared to graphene, which is rather preferred for digital circuit applications. A lot of effort has been recently dedicated to realize CNT digital ICs especially for flexible electronics applications [13]. On the other hand, graphene is expected to be rather suitable for analog device applications because of its features of no band-gap and extremely high mobility. Recently, several research oriented companies are running in a race to increase the f_T of wafer-scale graphene field-effect transistors (GFETs). As a consequence, various techniques using different substrates and graphene type have demonstrated promising results. For example, 100 GHz graphene transistors with 240 nm channel length have been demonstrated using epitaxial graphene on SiC substrate [14], and a f_T of 300 GHz has been achieved for an embedded back-gated graphene transistor on Si substrate using chemical vapor deposited (CVD) graphene [15,16]. Nevertheless, further improvement of graphene transistors on various key processes, such as top gate dielectrics and their alignments to reduce access resistance, etc., is necessary in order to catch up to the RF performance of III–V high-electron mobility transistors even before reaching their theoretically predicted performance [17].

It is critical to achieve low power dissipation and low voltage operation in order to avoid unacceptable power consumption and heat generation. Currently, several different device concepts have been proposed to realize ICs with a supply voltage below 0.5 V. In order to achieve low voltage operation, it is required to have sharp switching properties, which is expressed by the sub-threshold slope (SS) (mV/decade). The switching mechanism of conventional Si-MOSFETs is based on thermionic injection of the electrons over a barrier from the source to the drain, and a SS = 59.6 mV/decade at room temperature is theoretically the smallest value since the thermally activated electrons should follow Boltzmann distribution [4]. Since tunneling behavior is less sensitive to temperature, carrier injection based on tunneling is one of the potential solutions to achieve a small SS without a thermally induced smearing of the threshold voltage value [18]. The principle of operation of a p-type tunnel field-effect transistor (TFET) is depicted in Fig. 1 [19]. In the off-current state, the conduction level (hole reservoir) at the source is aligned to the energy gap of the channel region, and no hole can be injected into the channel region. In the on-state, the conduction level at the source is rendered below the valence level of the channel due to negative gate bias. The width of the barrier between the source and channel therefore becomes thinner as negative gate bias is increased. When an appropriate amount of gate voltage is applied, holes can thus be injected into the channel due to a Zener tunneling mechanism.

CNTs would be suitable for TFET applications because of their band structures and ballistic behavior [20]. Appenzeller et al. demonstrated SS of 40 mV/decade using CNT TFET although the on-state current is relatively small due to double barriers [21]. Zhang et al. reported that single-walled carbon nanotubes (SWCNTs) ambipolar tunneling devices exhibit SS down to 25 mV/decade [22]. Graphene may provide planar processing benefits because of its ideal two dimensional structure, and opening a bandgap can be achieved by forming a nanoribbon. Theoretically it is projected to have a SS as low as 0.19 mV/decade [23]. However, Graphene nanoribbons (GNRs) currently suffer from low carrier mobility and bandgap compared to theoretically predicted values due to severe carrier scattering at the rough edges of lithographically patterned GNRs [24]. One of the concerns on TFETs is potentially a small driving current because of tunneling. It is required to increase transmission probability across the interband tunneling barrier by selecting materials having a small energy barrier height (or energy bandgap) and effective mass of carriers. Additionally, high quality, high-κ gate dielectrics and excellent interfaces are required to effectively modulate the channel bands. Atomic layer deposition (ALD) of high-κ gate dielectrics needs to be developed to achieve small EOT and minimum interface trap density for TFET applications.

In addition to TFET concepts, various other devices, such as spin-FETs [25], mechanical switches [26] and bilayer pseudospin field-effect transistors (BiSFETs) [27], etc., have been proposed for replacing conventional CMOS devices for logic applications. Although, many of them are still at the stage of device concept development, scalable and high quality gate dielectrics are frequently required to realize the best device characteristics. For example, an ultrathin (<1 nm) low-κ

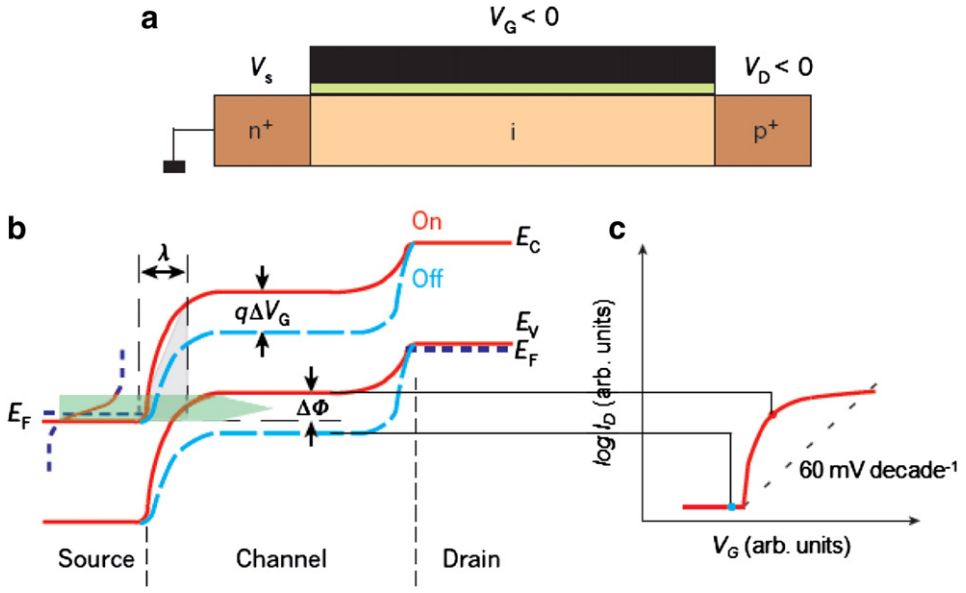

Fig. 1. Principle of operation of a p-type Tunnel FET (a) Schematic cross-sectional view, (b) energy band diagrams of p-i-n TFET for both on-state and off-state, (c) schematic curves of drain current as a function of gate voltage. TFET is expected to show SS < 60 mV/decade.
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